application report

E-Line Transistor Applications

Ferranti semiconductors

40p

Applications of the

E-Line Plastic Encapsulated Transistor

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CONTENTS

Introduction .. 3

Numerical List of Type Numbers .. 4

Section 1—Switching Characteristics of Transistors .. 5

Section 2—Astable Multivibrators .. 8
- (a) Edge Speed .. 9
- (b) Voltage Limitations .. 10
- The Current Mode Astable .. 12
- Serial Astable Circuits .. 14
- References .. 15
- Design Examples .. 16

Section 3—Monostable Multivibrators .. 20
- Simple Monostable .. 22
- Emitter-coupled Monostable .. 23
- Design Examples .. 24

Section 4—Bistables and Counters .. 27
- Binary Counters .. 30
- Ring Counters .. 32

Section 5—Digital Display Circuits and Digital to Analogue Converters .. 33
- Nixie Driver Circuit .. 33
- Counter .. 35
- Projection and Edge Illumination Readout .. 36
- 4-Bit Digital-to-Analogue Converter .. 37

Section 6—Ramp and Staircase Generators, Pulse Counters .. 38
- Constant Current Charge .. 38
- Boostrap Ramp Generator .. 39
- Parabolic Correction .. 40
- Feedback Integrator .. 41
- A Field Scan Generator for Vidicon Tubes .. 42
- A Wide Range Oscilloscope Timebase .. 43
- Staircase Generators .. 44
- Pulse Counters .. 45

Section 7—Schmitt Trigger Circuits .. 46
- High Speed Schmitt Trigger .. 47

Section 8—Stabilised Power Supplies .. 48
- A 12V, 1A Power Supply .. 49
- A 0–30V Variable Power Supply .. 52
- Operational Amplifier Power Supply .. 53

Section 9—Amplifier Circuits .. 54
- The Simple Amplifier .. 54
- Example of D.C. Design for a Single Stage Amplifier .. 55
- Feedback .. 56
- Wideband Linear R.F. Amplifier .. 57
- Wideband Current Amplifier .. 59
- Wideband Voltage Amplifier .. 60
- High Impedance, Unity Gain Amplifier .. 62

Section 10—Miscellaneous Circuits .. 64
- A.C. Millivoltmeter, Rectifier Stage .. 64
- A Millivoltmeter Pre-amplifier .. 65
- A Wide Range Wien Bridge Oscillator .. 66
- A Process Timer .. 68
- The Use of the Base-Emitter Junction of the ZTX300 as a Zener Diode .. 69
- Stable Voltage Reference Source .. 72
- A Chopper D.C. Amplifier .. 73

Section 11—Complementary Circuits .. 75
- Timing Relay Circuit .. 75
- Directly Coupled Amplifier .. 76
- A 150mW Audio Amplifier .. 77

Section 12—Avalanche Pulse Generator .. 79

General Information and Package Outlines .. 81

Publications Available .. 82

Customer Service Information .. 83

Introduction

This book is intended for engineers, students and amateurs who wish to gain basic working knowledge of circuits that may be unfamiliar to them or who wish to build experimental circuits or "one offs" with a minimum of trouble.

The design procedures given, in most cases, are simplified worst case. This will normally result in a circuit which cannot fail to operate. However, the reader's requirements will often differ in some details from the examples given and the conditions present at the input and output of the circuit will be unique to his own system. Thus, in most cases, it will be necessary for the reader to design a circuit to his own specification. The examples given will assist in this but the finished circuit should always be tested in breadboard form, preferably with worst case component values, to ensure that its operation is satisfactory.

This book covers a wide field and inevitably a lot has to be left out. However, we believe that everybody will find something of interest and many will find it a source of ideas and a stepping stone to a deeper understanding of electronic design.

Since the last edition of this book was first published, Ferranti have been undertaking a stringent exercise on the E-line range to qualify these products for BS 9000 approval. This exercise has been carried out in order to achieve the standards of quality and reliability necessary for the release of this product range to the appropriate British Standards Specification and where subjected to, and did survive without degregation, environmental tests which included:

1. *Rapid change of temperature, thermal shock in air.*

   Device cycled between −55 and +175°C for 400 times.

2. *Damp heat climatic test with reverse bias.*

   Device subjected to a relative humidity of 98% at a temperature of 55°C, collector/base reverse biased for 2,000 hours.

3. *Thermally accelerated test.*

   Device subjected to a temperature of 230°C with the collector-base and emitter-base reverse biased for a minimum duration of 160 hours.

It will be noticed that in the List of Type Nos., on Page 000, the BS approved types are available in two sub-categories, P & Q. The P category is the more stringent of the two in that the acceptance quality levels (AQL) are tighter, and certain environmental tests included in P are omitted in the Q category.

More detailed information on BS 9000, E-line reliability and E-line specifications is available on request from the Sales Department at Gem Mill.

It is important to note that all our E-line devices shown in the List of Type Nos. are manufactured with the same degree of care and process quality as those subject to the aforementioned BS 9000 qualification procedures.

NUMERICAL LIST OF TYPE NUMBERS

Where the approval for military use has been obtained, the appropriate British Standards registration is indicated in the column marked B.S. number

Type	Pro-electron number	B.S. number			Uses (see notes below)	Type	Pro-electron number	B.S. number			Uses (see notes below)
			Category P	Category Q					Category P	Category Q	
	BFS59	9365	F096	F099	A	ZTX337					A,M
	BFS60	9365	F097	F100	A	ZTX338					A,M
	BFS61	9365	F098	F101	A	ZTX341	BSV28	9365	F054	—	K
	BFS96	9365	F082	F085	B	ZTX342	BSV29	9365	F055	—	K
	BFS97	9365	F083	F086	B						
	BFS98	9365	F084	F087	B	ZTX382					A,G
ZDX1F/R					O	ZTX383					A,G
ZDX2F/R					O	ZTX384					A,G
ZDX3F/R					O	ZTX450		9365	F137	F139	A,M
ZDX4F/R					O	ZTX451		9365	F138	F140	A,M
ZTX107		9365	F028	—	A	ZTX500	BCW11	9365	F031	—	B
ZTX108		9365	F029	—	A	ZTX501	BCW13	9365	F032	—	B
ZTX109		9365	F030	—	A	ZTX502	BCW15	9365	F033	—	B
ZTX114					G	ZTX503	BCW17	9365	F034	—	B
ZTX180					I	ZTX504	BCW19	9365	F035	—	B
ZTX181					I	ZTX510	BSV33				F
ZTX196					I	ZTX530	BCW21				H
ZTX197					I	ZTX531	BCW23				H
ZTX212		9365	F130	—	B,D	ZTX537					B,N
ZTX213		9365	F131	—	B,D	ZTX538					B,N
ZTX214		9365	F132	—	B,D	ZTX541					L
ZTX223					A	ZTX542					L
ZTX237					A,G	ZTX550		9365	F143*	F145*	B,N
ZTX238					A,G	ZTX551		9365	F144*	F146*	B,N
ZTX239					A,G	ZTX3702					B
ZTX300	BCW10	9365	F072	F077	A	ZTX3703					B
ZTX301	BCW12	9365	F073	F078	A	ZTX3704					A
ZTX302	BCW14	9365	F074	F079	A	ZTX3705					A
ZTX303	BCW16	9365	F075	F080	A	ZTX3706					A
ZTX304	BCW18	9365	F076	F081	A	ZTX3707					G
ZTX310	BSV23	9365	F040	—	E	ZTX3708					A
ZTX311	BSV24	9365	F041	—	E	ZTX3709					A
ZTX312	BSV25	9365	F042	—	E	ZTX3710					A
ZTX313	BSV26	9365	F043	—	E	ZTX3711					A
ZTX314	BSV27	9365	F044	—	E	ZTX3903					A,C,G
ZTX320	BFW97	9365	F088	F090	J	ZTX3904					A,C,G
ZTX321		9365	F089	F091	J	ZTX3905					B,D,H
ZTX325		9365	F102	F104	J	ZTX3906					B,D,H
ZTX326		9365	F103	F105	J	ZTX4400					A,C
ZTX327					J	ZTX4401					A,C
ZTX330	BCW20	9365	F092	F094	G	ZTX4402					B,D
ZTX331	BCW22	9365	F093	F095	G	ZTX4403					B,D

*Indicates approval pending

NOTES: A General Purpose, n-p-n
B General Purpose, p-n-p
C Medium Speed Switching, n-p-n
D Medium Speed Switching, p-n-p
E High Speed Switching, n-p-n
F High Speed Switching, p-n-p
G Low Noise, n-pn-
H Low Noise, p-n-p
I Television, n-p-n
J VHF/UHF, n-p-n
K High Voltage, n-p-n
L High Voltage, p-n-p
M High Dissipation, n-p-n
N High Dissipation, p-n-p
O Double Diodes

SECTION 1

SWITCHING CHARACTERISTICS OF TRANSISTORS

In most switching circuits trigger capacitors are required to differentiate pulses and provide d.c. isolation between stages, and speed-up capacitors are required to neutralize the stored charge and junction capacitances of the transistors. In most cases it is sufficient to choose values small enough not to interfere with the operation of the circuit at its maximum frequency. These capacitors do however have minimum values depending on the type of transistor used, its collector and base currents and the amplitudes of the waveforms involved.

In order to understand the need for speed-up capacitors consider the simple inverter circuit shown in Figure 1.1.

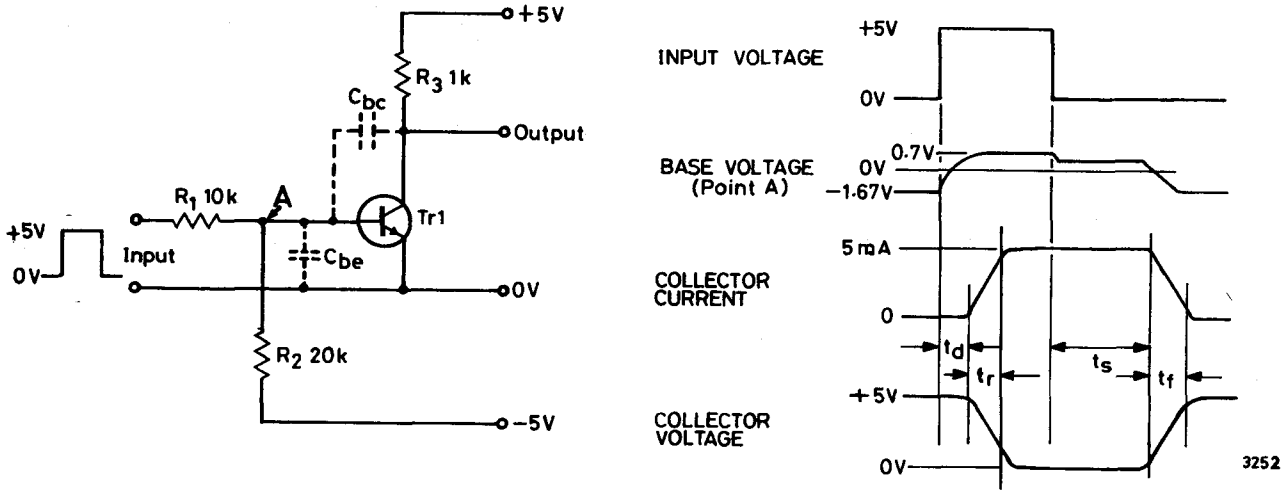


Figure 1.1. Simple inverter circuit and switching waveforms.

Initially Tr1 is cut off with its base-emitter junction reverse biased to –1·67 volts and its collector-base junction reverse biased by 6·67 volts. When the input pulse arrives the potential at point A rises exponentially as the junction capacitances of the transistor charge, until point A reaches +0·7V and the base-emitter junction of the transistor starts to conduct. The time taken for this to occur is called the delay time (t_d). As the base current flows, charged carriers begin to accumulate in the base region and the collector current increases in proportion until it is limited by the collector load resistance R3. The time taken for the collector current to increase from 10% of its final value to 90% of its final value is called the rise time (t_r). As the collector voltage approaches zero the collector-base junction becomes forward biased and conducts the excess base current. The base now starts acting as an emitter and begins to inject charge carriers into the collector. This causes a considerable accumulation of charge in the collector region which must be removed, either by recombination or by reverse base current, before the transistor can begin to turn off. The time taken for this excess charge to be removed is called the storage time (t_s), and during this time the transistor remains saturated. At the end of the storage time all excess charge carriers have been removed and the base charge is simply that required to maintain collector current. As this charge is reduced further the collector current falls in sympathy until transistor is cut off. The time taken for the collector current to fall from 90% to its previous value to 10% of its previous value is called the fall time (t_f).

Due to the low leakage currents of silicon transistors it is not usually necessary to reverse bias the base to ensure d.c. stability. This reduces delay time but causes a large increase in both the storage time and fall time since the charge can only be dissipated by recombination instead of by the reverse base current provided by R2. This can be overcome by connecting a capacitor in parallel with R1 so that the charge stored on the "speed up" capacitor is sufficient to neutralize the total charge in the conducting transistor, i.e. the base charge, the collector storage charge and the junction capacitances. Figure 1.2 shows the effect of varying this capacitor from zero to a critical value at which all the charge is just removed. This value depends on three factors: (a) the transistor type, (b) the base and collector currents, and (c) the amplitude of the input pulse. As no stored charge information is available for E-Line transistors it is necessary for the minimum values to be determined experimentally, preferably in a worst case version of the actual circuit. However as a guide, the minimum values of charge necessary to turn off devices of the ZTX300/500, ZTX310/510 and ZTX107 series have been plotted for various d.c. conditions in Figure 1.3.

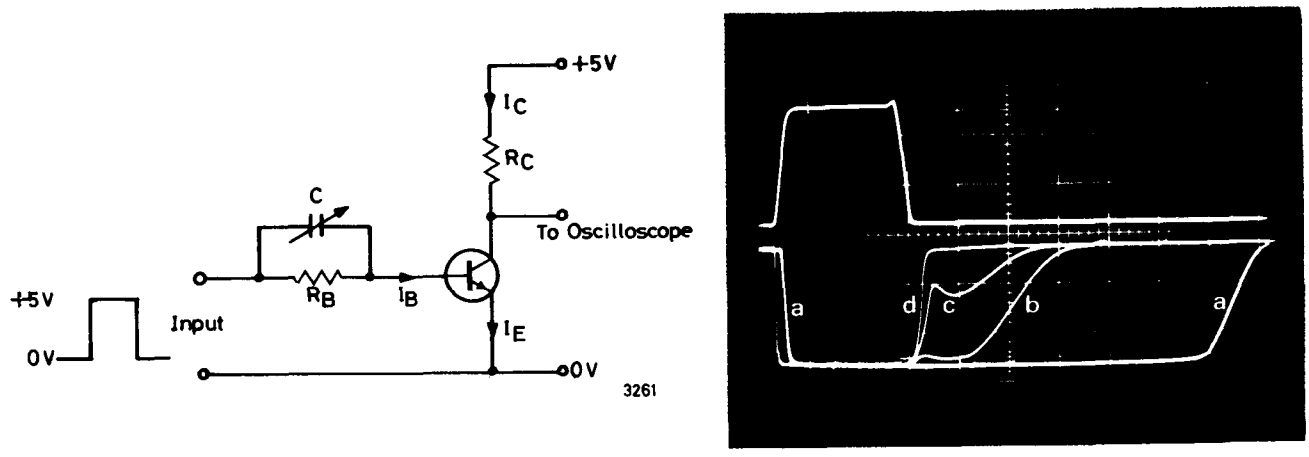


Figure 1.2. Circuit for measuring stored charge, with waveforms.

Upper trace—Input waveform

Lower traces—(a) C = 0
(b) C = 100pF
(c) C = 120pF
(d) C = 130pF (stored charge just removed)

Horizontal scale: 0·2μS/cm
Vertical scale: 2V/cm
ZTX300, I_B = 1mA
I_C = 10mA

Note the reduction in delay time from trace "a" to traces "b, c, d".

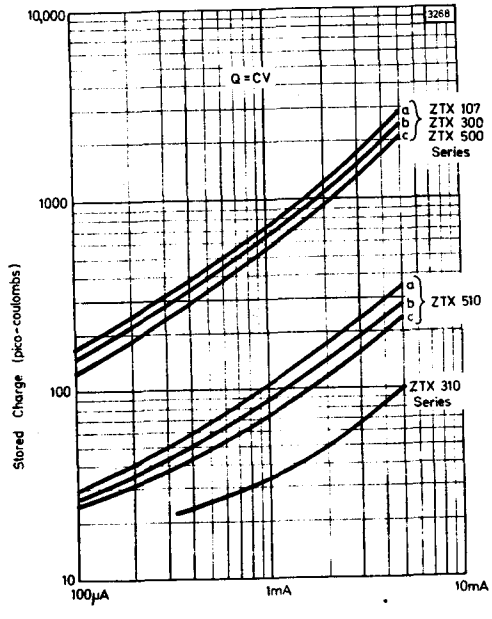


Fig. 1.3

Stored charge versus base current for ZTX107/300/500/310/510 devices.

Curves marked (a) I_C/I_B = 10
(b) I_C/I_B = 20
(c) I_C/I_B = 40

There was no significant difference for ZTX310 series transistors.

The circuit used for measuring the minimum values of trigger charge and the results obtained are shown in Figures 1.4 and 1.5. The values obtained are higher than the above case because the trigger capacitor not only has to remove all the stored base charge, but also has to overcome the d.c. bias provided by Rb.

In a practical circuit there will usually be steering diodes and resistors or other circuit components, which will absorb a proportion of the trigger charge. Consequently it will usually be necessary to use a higher value of trigger capacitance than is suggested by the curves, which should be treated only as a guide. It is always advisable to measure the values under working conditions in a breadboard circuit built with worst case component values.

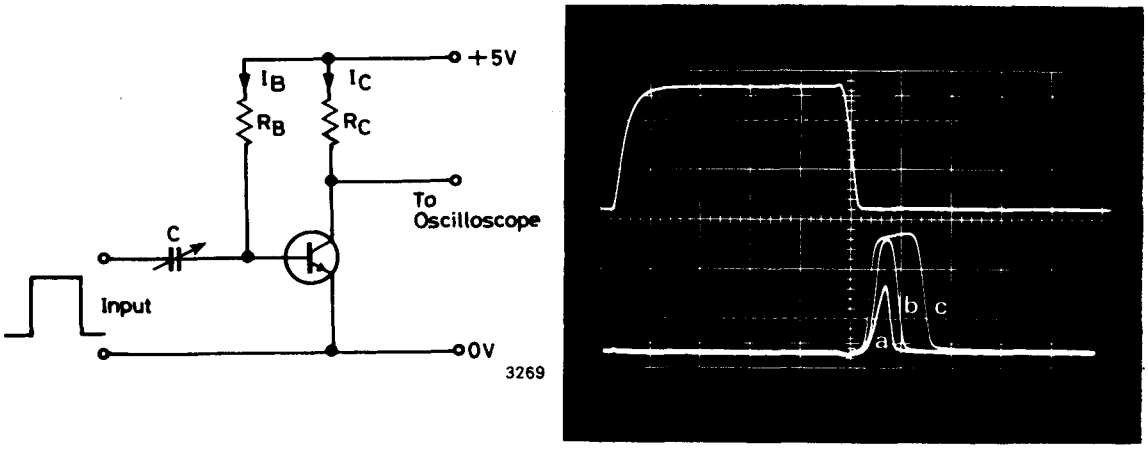


Figure 1.4. Circuit for measuring minimum trigger charge, with waveforms.

Upper trace—Input waveform.

Lower traces—Output waveforms with trace (a) Variable capacitor "C" below critical value.
(b) "C"at critical value with collector voltage rising to 90% of final value.
(c) "C" above critical value.

Horizontal scale = 0·2μS/cm; Vertical scale scale 2V/cm; ZTX300, I_B = 1mA, I_C = 10mA.

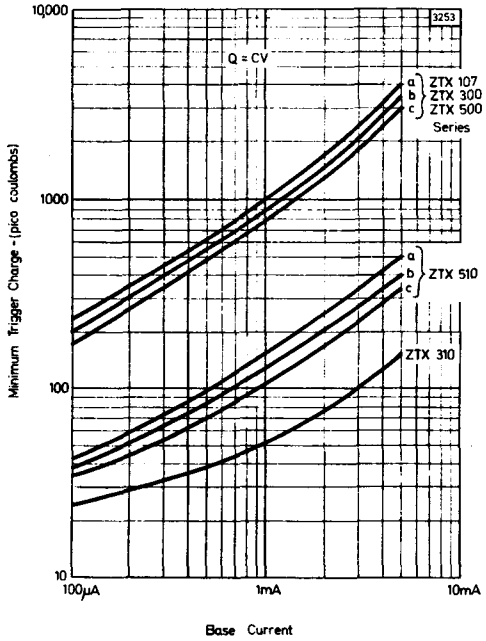


Figure 1.5

Minimum trigger charge versus base current for ZTX107/300/500/310/510 series devices.

Curves marked (a) I_C/I_B = 10
(b) I_C/I_B = 20
(c) I_C/I_B = 40

Only the highest figure has been recorded for ZTX310 as differences were small.

It should be pointed out that these measurements were taken from the worst samples out of a batch of fifty and as these parameters are not tested during manufacture no guarantee can be given that future production will conform to these results.

The transient behaviour of transistors is a complex subject and this summary has, of necessity, been greatly simplified. The following books are recommended for further study:

(1) Dakin & Cooke. Circuits for Digital Equipment. Iliffe (1967).
(2) Motorola. High Speed Switching Transistor Handbook (1963).

SECTION 2

ASTABLE MULTIVIBRATORS

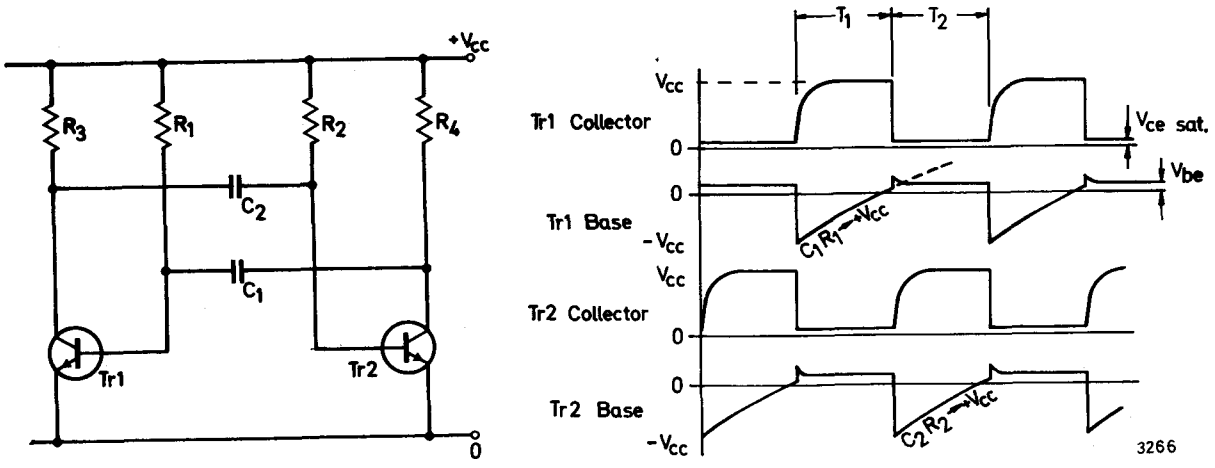
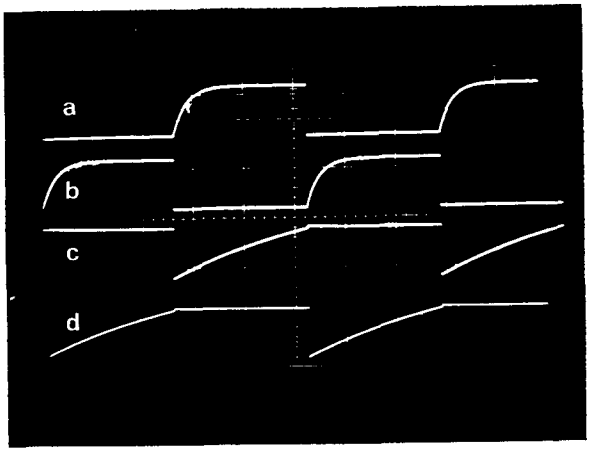


Figure 2.1. Basic Astable.

Typical component values: R1 = R2 = 15kΩ
R3 = R4 = 1kΩ
C1 = C2 = 0·047μF
Tr1 = Tr2 = ZTX300
+ V_{cc} = 5 volts



Oscilloscope trace
(a)—Tr1 collector
(b)—Tr2 collector
(c)—Tr1 base
(d)—Tr2 base

Frequency = 963Hz (measured).

The astable multivibrator (Figure 2.1) is basically an a.c. coupled two stage amplifier with phase inversion over each stage and with the output coupled back to the input. This positive feedback causes the circuit to oscillate continuously between two quasi-stable states. Suppose that Tr1 has just turned on and Tr2 is off. The voltage at the base of Tr2 rises exponentially towards the supply voltage as C2 charges through R2 until it reaches +0·7V, when Tr2 starts to conduct. The collector voltage of Tr2 starts to fall and this change is coupled through C1 to the base of Tr1. Tr1 now begins to turn off and its collector voltage rises, increasing the base current of Tr2 and further reducing its collector voltage. This regenerative action results in very rapid switching from the "off" state to the "on" state and vice-versa. The regenerative action ceases when Tr2 saturates. Tr1 is now completely cut off with its base reverse biased by (approximately) $-V_{cc}$. The potential of Tr1 base now rises exponentially with a time constant of (C1 × R1) as C1 charges towards the supply voltage ($+V_{cc}$). As the voltage at Tr1 base reaches +0·7V, Tr1 switches on, Tr2 is cut off and the cycle repeats.

If the transistor leakage currents are ignored and the collector saturation voltage and base-emitter "on" voltage are assumed to be zero, simple approximate formulae for the periods T1 and T2 may be derived as follows:

The instantaneous base voltage of T1, $V_{b1} = 2V_{cc}\left[1-e^{-\frac{t}{C_1R_1}}\right] - V_{cc}$

$$= V_{cc}\left[1-2e^{-\frac{t}{C_1R_1}}\right]$$

For $V_{b1} = O$ $\quad 2e^{-\frac{t}{C_1R_1}} = 1.$

$t = T1 = C_1R_1 \log_n 2$

i.e.: $T1 = 0.693\ C_1R_1$ 2.1

similarly $T2 = 0.693\ C_2R_2$

$T = 0.7CR$ is a useful approximation.

These formulae are sufficiently accurate for most practical purposes, but where a more precise estimate is required V_{cc}, V_{be} and $V_{ce(sat)}$ must be taken into account. T1 and T2 can be expressed more accurately as:

$$T1 = C_1R_1 \log_n \frac{2V_{cc} - V_{be} - V_{ce(sat)}}{V_{cc} - V_{be}} \quad \text{.....2.2}$$

and similarly for T2.

For the circuit shown in Figure 2.1 the frequency calculated from equation 2.1 is 1·022kHz Assuming $V_{be} = 0{\cdot}7V$ and $V_{cc(sat)} = 0{\cdot}1V$ equation 2.2 gives – $T_1 = T_2 = C_1R_1 \log_n \frac{10-0{\cdot}7-0{\cdot}1}{5-0{\cdot}7}$

$$= C_1R_1 \log_n 2.14$$

$$= 0.047\ .\ 10^{-6}\ .\ 15.10^3\ .\ 0.761 \text{ secs.}$$

$T1 = T2 = 0.536mS$

Hence the total period is 1.072mS and the frequency is 934Hz. The frequency measured on the actual circuit was 963Hz with 1% components.

The maximum values of R1 and R2 are limited to h_{FE} . R3 and h_{FE} . R4 respectively, where h_{FE} is the minimum d.c. current gain of the transistors used. In practice it is advisable to use a value somewhat lower than this to ensure that the transistor is fully saturated.

The minimum values of R1 and R2 must be such as to allow the collector voltage to complete its full excursion during the pulse period. Referring to Figure 2.1, for Tr1 collector to recover to at least $0{\cdot}98V_{cc}$, T1 must be at least equal to $4C_2R_3$ since $(1-e^{-4}) = 0{\cdot}98$.

Hence $T1 = 0{\cdot}69\ C_1R_1 \geqslant 4\ .\ C2R3.$

if C1 = C2, $R1 \geqslant 5.8R3$

and $R2 \geqslant 5.8R4$ 2.3

If recovery to $0{\cdot}99\ V_{cc}$ is required these become:

$R1 \geqslant 6.7R3$

$R2 \geqslant 6.7R4$ 2.4

The basic astable multivibrator as described so far has two disadvantages which can, where necessary, be overcome by modifications to the circuit.

(a) Edge Speed

The positive going edge of the collector waveform is slow because the timing capacitor has to re-charge through the collector load resistor. This can be avoided by providing a separate re-charge path for the timing capacitor as shown in Figure 2.2. When Tr2 turns off the diode is reversed biased and the collector voltage rises rapidly to V_{cc} whilst the voltage at point A rises exponentially with time constant C1 . R5 as C1 recharges. When Tr2 turns on the diode becomes forward biased and R4, R5 appear effectively in parallel. It is usually convenient for the values of R4 and R5 to be equal but this is not important so long as R5 is sufficiently small to completely recharge C1 in the period that Tr2 is turned off. The technique can of course be applied to both sides of the multivibrator when clean waves are required at both outputs.

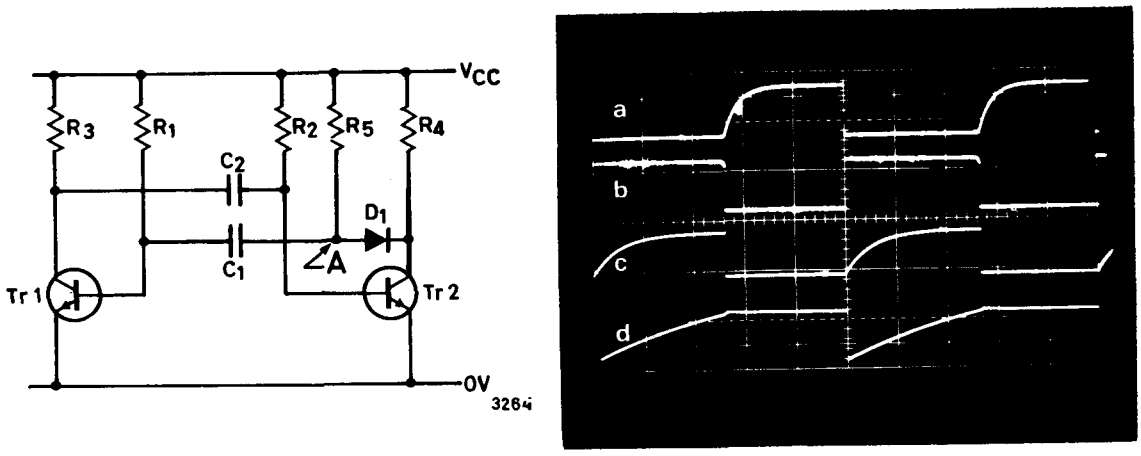


Figure 2.2. Astable modified for improved waveform.

Typical component values:

R1 = R2 = 15kΩ
R3 = 1kΩ
R4 = R5 = 2k2
C1 = C2 = 0·047μF
Tr1 = Tr2 = ZTX300
D1 = ZS140
$+V_{cc}$ = 5 volts

Frequency = 1·066kHz (measured)

Trace (a) Tr1 collector
(b) Tr2 collector
(c) Point "A"
(d) Tr2 base

(b) Voltage Limitations

In the basic multivibrator (Figure 2.1) the transistor base is momentarily reverse biased to $-V_{cc}$. This limits the maximum value of V_{cc} to the base-emitter breakdown voltage of the transistor (usually 5V). This is too low for many applications but higher supply voltages can be used if the transistor is protected against base-emitter breakdown. Two circuits which do this are shown in Figures 2.3 and 2.4.

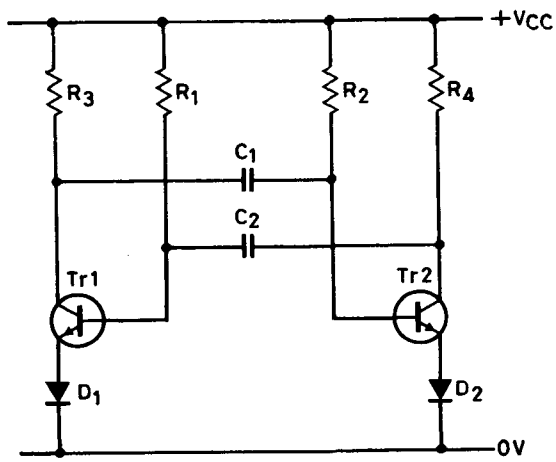


Figure 2.3

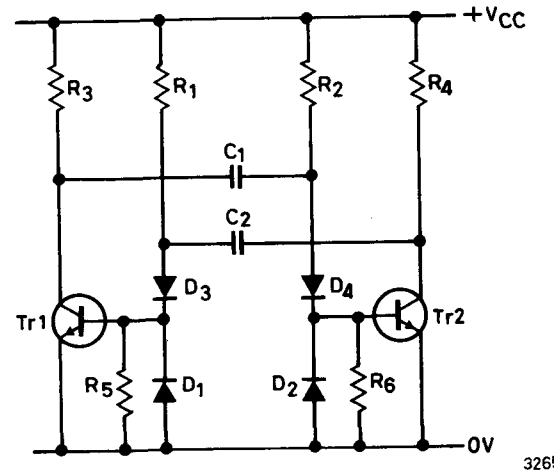


Figure 2.4

Typical component values:

R1 = R2 = 15kΩ
R3 = R4 = 1kΩ
C1 = C2 = 0·047μF
Tr1 = Tr2 = ZTX300
D1 = D2 = ZS140
Frequency = 1kHz
V_{cc} = 12V max.

Typical values are as Figure 2.3 except:

D3 = D4 = ZS120
R5 = R6 = 10kΩ
V_{cc} = 25V max.

In the circuit of Figure 2.3 diodes D1 and D2 become reverse biased when the base of the transistor is driven negative and prevents any current from flowing in the base-emitter junction. The diodes should preferably be high speed types such as ZS140 and the transistors chosen must have a collector-base breakdown voltage (V_{cbo}) of at least twice V_{cc}, since the collector is at $+V_{cc}$ when the base is reverse biased to $-V_{cc}$.

The maximum value of V_{cc} in the circuit of Figure 2.4 is limited to the collector-emitter breakdown voltage (V_{ceo}) of the transistor since diodes D3 and D4 completely isolate the transistor bases. In this circuit it is often advantageous for diodes D1 and D2 to be fast types (e.g. ZS140) and diodes D3 and D4 to be slow types (e.g. ZS120) as the stored charge in D3, D4 helps to turn the transistors off rapidly. At low speeds diodes D1 and D2 can be omitted if fast diodes are used for D3 D4.

Another technique which is particularly useful at high repetition rates is to "catch" the collector voltage at 5V by means of diodes D1 and D2 and zener diode D3, as shown in Figure 2.5. In this case the collector voltage swing, and hence the reverse bias applied to the base, is limited to 5V and the collector waveform is considerably improved. It should be noted however that the simplified formulae derived earlier no longer apply and the component values required must be calculated from first principles.

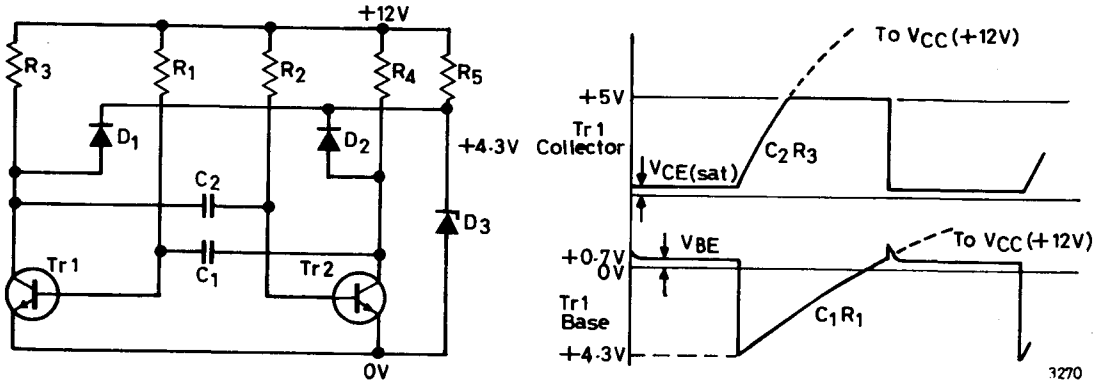
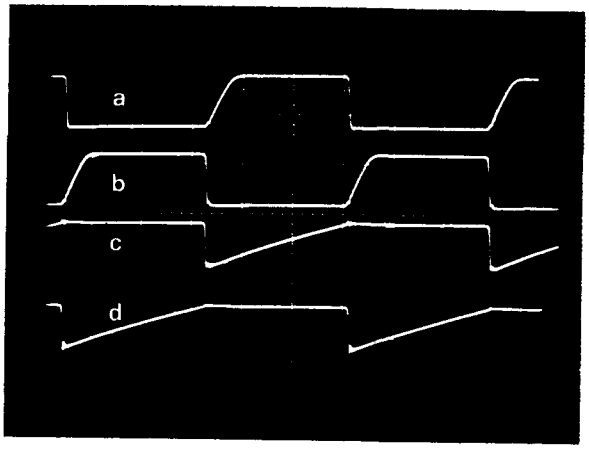


Figure 2.5. Astable with catching diodes.

Typical component values:

R1 = R2 = 10kΩ
R3 = R4 = 1kΩ
R5 = 4k7
C1 = C2 = 150pF
Tr1 = Tr2 = ZTX311
D1 = D2 = ZS140
D3 = KSO43A
Frequency ≈ 1MHz (903 kHz measured)
V_{cc} = +12V



Oscilloscope trace (a)—Tr1 collector
(b)—Tr2 collector
(c)—Tr1 base
(d)—Tr2 base

Horizontal scale = 200nS/cm., vertical scale = 5V/cm.

All these circuits can of course be used with p-n-p transistors if all diodes and the supply voltage are reversed. All the waveforms produced will also be inverted. Many of the techniques described here can also be applied to monostables.

The types of astable multivibrator described so far are the most generally used but there are other types which are useful in some circumstances.

The Current Mode Astable

In this circuit the transistors do not saturate. This greatly reduces the stored charge and enables the circuit to operate at much higher repetition rates than are possible with the simple saturating astable. The basic circuit is shown in Figure 2.6.

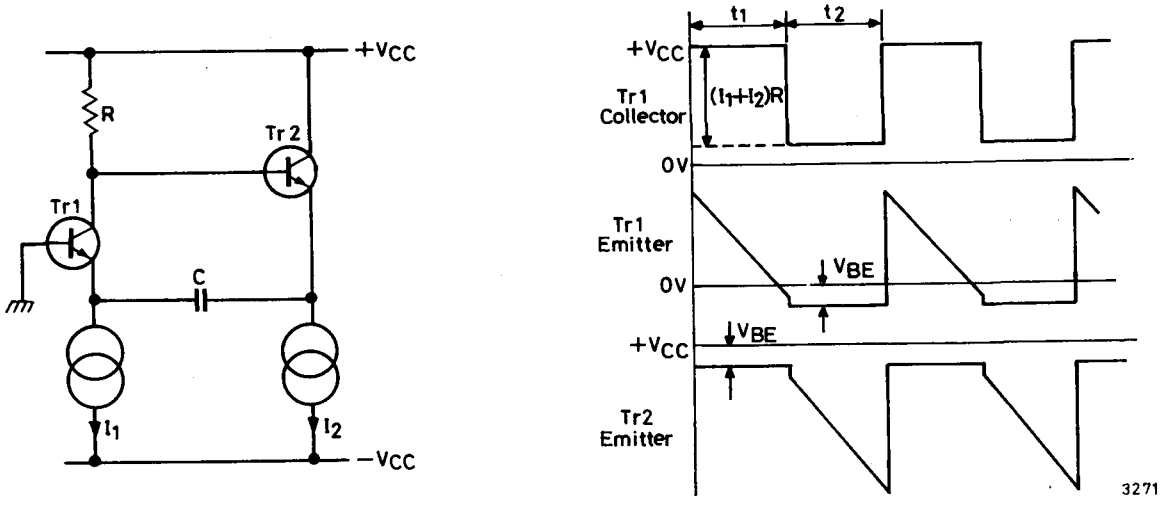


Figure 2.6. Basic Bowes Astable.

Assume that Tr1 has just been turned off and Tr2 is on. The potential at Tr1 emitter falls linearly as C charges with I_1 until the emitter reaches –0·7V when Tr1 starts to conduct. The collector voltage of Tr1 starts to fall and Tr2 is reversed biased. Both current sources I_1 and I_2 now flow into the emitter of Tr1 causing a voltage drop of $(I_1 + I_2)$. R across the collector load resistor. This voltage drop must not be sufficient to saturate Tr1. The voltage at Tr2 emitter now falls linearly as C discharges with I_2 until it reaches 0·7V below the collector voltage of Tr1. Tr2 then starts to conduct, the current flowing into Tr1 emitter is reduced and the collector voltage of Tr1 rises until Tr1 is completely cut off and Tr2 is conducting I_1 and I_2. The cycle then repeats. Timing equations can be derived as follows, assuming that the transistor common base current gain is unity, and the leakage currents and V_{be} can be neglected.

$$\text{Voltage drop } V_1 = (I_1 + I_2) \,.\, R = \frac{I_1 t_1}{C} = \frac{I_2 t_2}{C}$$

(since CV = IT)

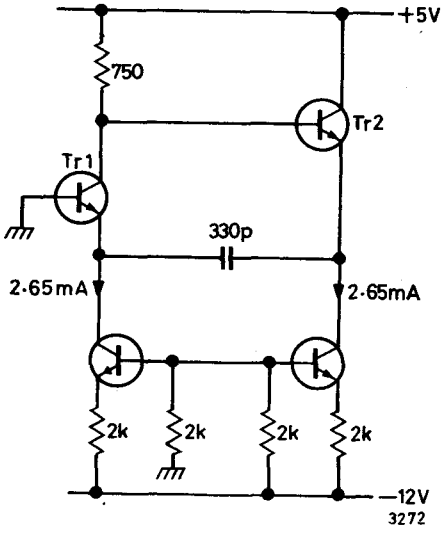
$$\text{therefore } t_1 = \frac{(I_1 + I_2)\,CR}{I_1} \text{ and } t_2 = \frac{(I_1 + I_2)\,CR}{I_2}$$

$$\text{hence the total period } t_1 + t_2 = \frac{(I_1 + I_2)^2\,CR}{I_1 I_2}$$

$$\text{if } I_1 = I_2 \text{ then } t_1 + t_2 = 4CR \qquad \text{2.5}$$

$$\text{or if } \frac{I_1}{I_2} = n, \text{ for unequal currents, } t_1 + t_2 = \frac{(1 + n)^2\,CR}{n} \qquad \text{2.6}$$

A practical circuit is shown in Figure 2.7 together with the waveforms obtained. Figure 2.8 shows the effect of replacing the current sources with resistors delivering the same average currents. As can be seen, there is some degradation of the waveform and the frequency is increased due to the exponential charging.



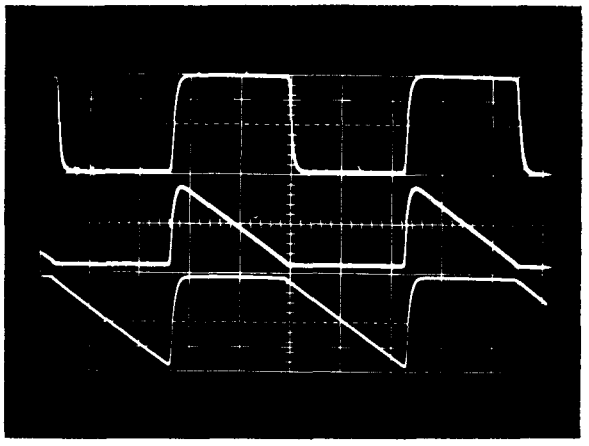
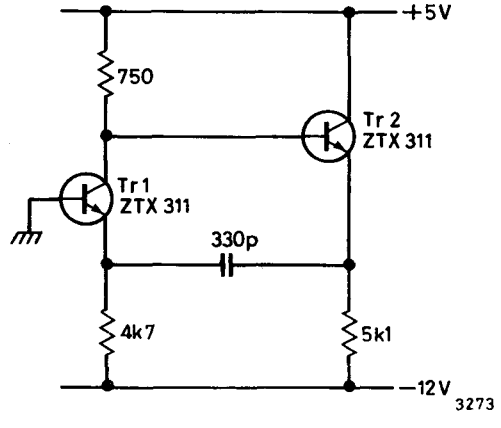


Figure 2.7

Practical circuit for 1MHz
All transistors—ZTX311
Measured frequency—1·09MHz

Upper trace, Tr1 collector
Centre trace, Tr1 emitter
Lower trace, Tr2 emitter
Vertical scale: 2V/cm
Horizontal scale: 200nS/cm



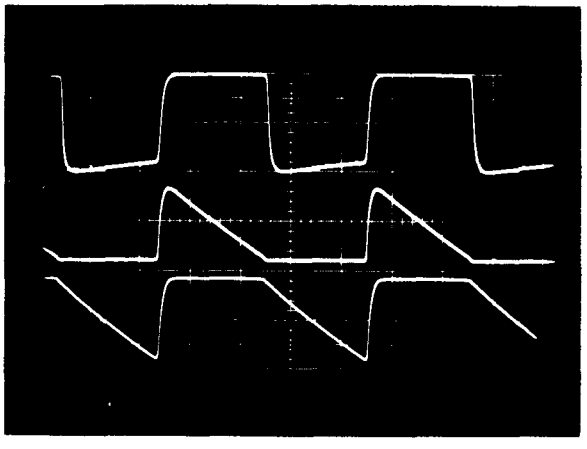
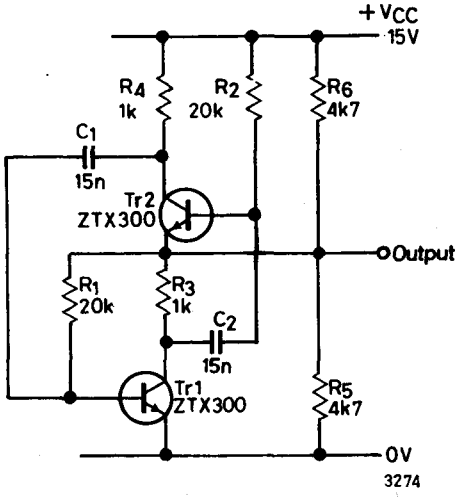


Figure 2.8. Bowes astable with resistor current sources. f = 1232kHz.

Serial Astable Circuits

Serial type astables, in which the two transistors are connected in series, have been described by various authorities. In most cases the design has been aimed at obtaining a better output waveform than that provided by the conventional astable.



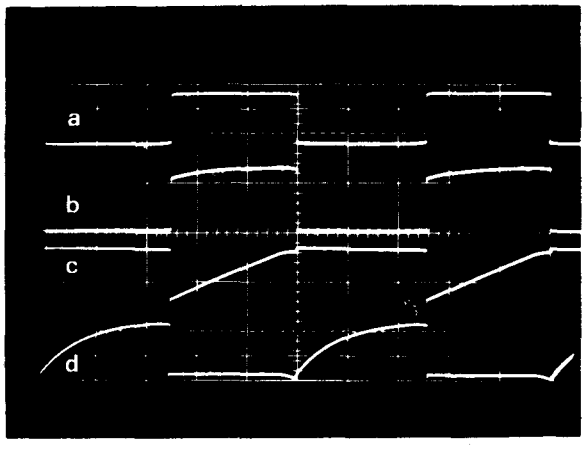
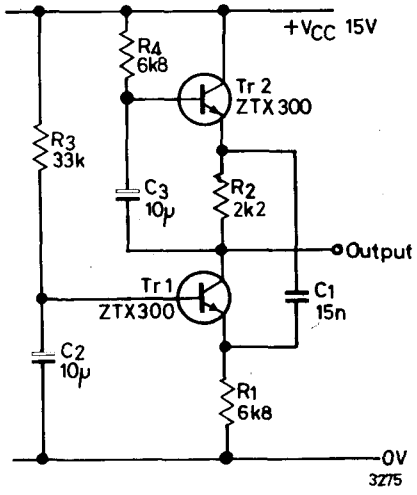


Figure 2.9. Modified Smith astable, with waveforms.

$f_{..}$ = 10kHz

Trace (a)—Output
(b)—Tr1 collector (10V/cm)
(c)—Tr1 base
(d)—Tr2 collector (2V/cm)

Figure 2.9 shows a slightly modified version of the Smith astable (ref. 2). With ZTX300 series transistors the circuit will oscillate up to 100kHz, and to over 1MHz with ZTX310 series devices. The transition times are approximately 50nS on both edges. Output voltage swing with a 15V supply is approximately 10V pk-pk, the lower level being 2·5V and the upper level 12·5V. Frequency of oscillation with the component values shown $= \frac{3}{CR}$. R1 and R2 are the timing resistors.



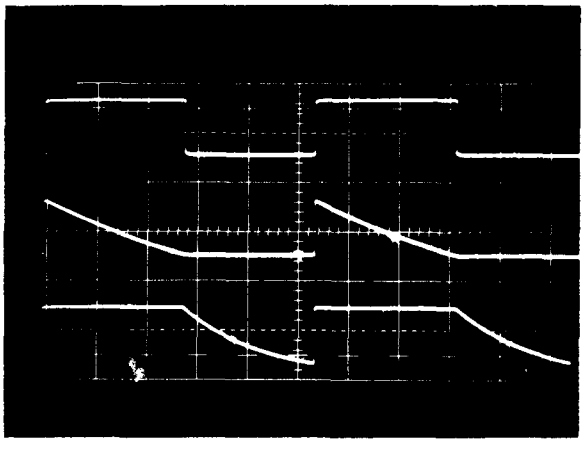


Figure 2.10. Ristic astable, with waveforms.

C2 and C3 are decoupling capacitors.

$f_{..}$ = 9kHz.

Upper trace—output
Centre trace—Tr1 emitter
Lower trace—Tr2 emitter
Vertical scale = 5V/cm
Horizontal scale = 20µS/cm

Figure 2.10 shows a serial astable due to Ristic (ref. 3). The performance of this is similar to the Smith circuit except that the output voltage swing is reduced to about 5V with a 15V supply. Edge speeds are approximately 100nS and the frequency of oscillation is given by $f_o = \frac{1{\cdot}35 \times 10^{-4}}{C.}$ with the components values shown in Figure 2.10.

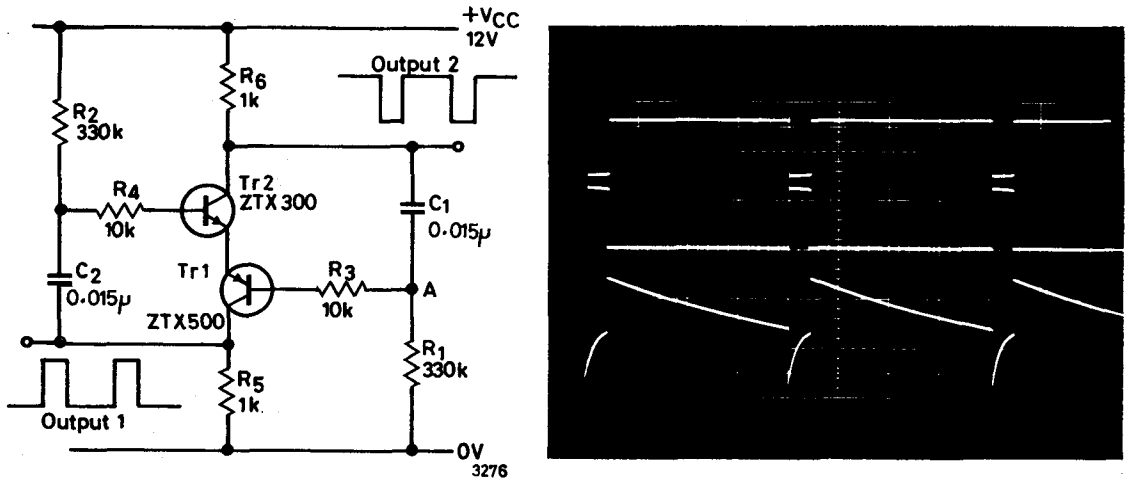


Figure 2.11. Ho astable, with waveforms.

Upper trace—Output 2
Centre trace—Output 1
Lower trace—Point A
} Vertical scale—5V/cm
Horizontal scale—1mS/cm

Figure 2.11 shows a complementary serial astable due to Ho (ref. 4). Very large mark-space ratios are possible with this circuit which has two identical but complementary outputs. The pulse period is not well defined since it depends on the transistor h_{FE} but the period between the pulses is given by the normal astable formula; i.e. T = 0·7CR. It is important that the base current provided by R1, R2 should *not* be sufficient to saturate the transistors or latch-up occurs.

References

(1) Dakin, C. J., and Cooke, C. E. G Circuits for Digital Equipment. Iliffe.

(2) Smith, J. H. Multivibrator Circuits, Electronic Engineering 35, 46. (1963).

(3) Ristic, V. M. A new type of Free Running Multivibrator, Electronic Engineering. 36, 232 (1964).

(4) Ho, C. F. Dual Polarity Astable Multivibrator, Electronic Engineerinng 41, 230 (1969).

Design Examples

Worst Case Design

The following factors should be remembered when performing a worst case design.

(a) The V_{be} of a silicon transistor falls by approximately 2mV for every 1°C increase in temperature.

(b) The h_{FE} of a silicon transistor rises by approximately 0·7% for every 1°C increase in temperature.

(c) Depending on the conditions of use the value of a resistor will change with time due to the effects of soldering, moisture and ageing, and may go outside its nominal tolerance. A moulded carbon resistor may change by 20% from its original value, a carbon film resistor by 5% and a metal oxide resistor by 1%. In the examples given it will be assumed that a 10% resistor will have an ultimate tolerance of 20%, etc.

Example 1

A 1kHz square wave astable to operate from a 5V ±10% supply. No d.c. load, but output impedance of 1kΩ. Ambient temperature −10°C to +50°C. (Circuit and waveforms shown in Figure 2.1).

(1) Choose transistor type ZTX300.

(2) Choose collector load resistor. 1kΩ nominal ±20%.

(3) Minimum supply voltage is the worst condition for turning the transistor fully on. With 4·5V d.c. supply, collector current = 4·5mA nominal.

= 5·6mA maximum with R3, R4 20% low.

(4) Minimum current gain of ZTX300 at 5·6mA = 45 at 25°C.

= 34 at −10°C.

Hence the minimum base current to saturate $= \frac{5{\cdot}6}{34} = 0{\cdot}165$mA with base resistor 20% high.

(5) From ZTX300 curves, V_{be} at −10°C = 0·8V.

Hence the minimum value of base resistor R1, R2 $= \frac{4{\cdot}5-0{\cdot}8}{0{\cdot}165} \times \frac{100}{120}$

i.e. Maximum value of R1, R2 = 18·7kΩ.

(6) The minimum value of R1, R2 to ensure recovery of the collector voltage to $0{\cdot}99V_{cc}$ = 6·7kΩ (from equation 2.4). Any value of timing resistor R1, R2 between these two limits will be suitable. For a 1kHz square wave output both periods T1 and T2 must be 0·5mS.

$T = 0.7CR$, therefore $CR = \frac{0{\cdot}5}{0{\cdot}7} = 0{\cdot}7$mS.

The above conditions are satisfied if R1 = R2 = 15kΩ.

C1 = C2 = 0·047μF.

Example 2

An astable to generate a 100μS pulse with a repetition time of 1mS. Other conditions as example 1.

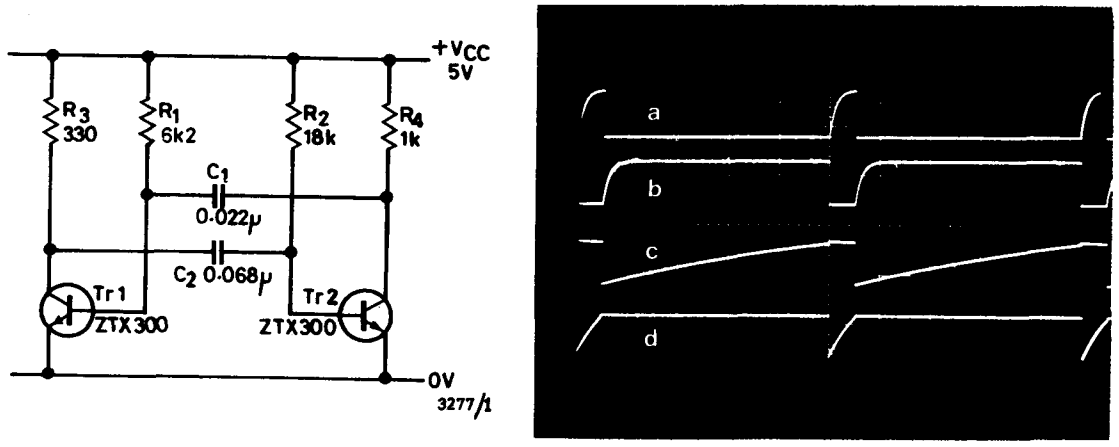


Figure 2.12

Trace (a)—Tr1 collector
(b)—Tr2 collector
(c)—Tr2 base
(d)—Tr1 base
} Vertical scale: 5V/cm
Horizontal scale: 200μS/cm

(1) Choose transistor type ZTX300.

(2) Choose load resistor R4. 1kΩ ±20%.

(3) (4) (5) Maximum value of R2 = 18·7kΩ (as example 1).

(6) Tr2 is held off for 900μS. Therefore time constant C2R2 = $\frac{900}{0{\cdot}7}$ = 1280μS.

A reasonable approximation to this is obtained if R2 = 18kΩ. C2 = 0·068μF.

(7) R3 must be able to fully recharge C2 during the 100μS pulse. From equation 2.3; for recovery to 98% of the supply voltage.

$$R1C1 > 5{\cdot}8\ R3C2.$$

but $R1C1 = \frac{R2C2}{9}$ since a 100μS pulse is required from Tr1.

therefore $R3 < \frac{R2}{5{\cdot}8 \times 9} = \frac{18k}{52} = 350\Omega.$

The nearest preferred value below this is 330Ω.

(8) Worst case collector current of Tr1, with 4·5V supply = $\frac{4{\cdot}5}{330} \times \frac{100}{80}$ = 18·7mA.

minimum current gain of ZTX300 at 18·7mA = 54 at 25°C.
= 40 at −10°C.

therefore minimum base current to saturate = $\frac{18{\cdot}7}{40}$ = 0·47mA with R1 20% high.

(9) Maximum value of R1 = $\frac{4{\cdot}5 - 0{\cdot}8}{0{\cdot}47} \times \frac{100}{120}$ = 6·6kΩ.

(10) Minimum value of R1, $R2C2 > 5{\cdot}8\ R4C1$

$$9\ R1C1 > 5{\cdot}8\ R4C1$$

therefore $R1 > \frac{5{\cdot}8R4}{9} = 650\Omega.$

However a value as low as this would be undesirable since it would impose an additional load on Tr2.

For a 100μS pulse $C1R1 = \frac{100}{0{\cdot}7}$ = 140 μS.

A reasonable approximation to this is obtained with R1 = 6k2, C1 = 0·022μF.

The finished circuit and output waveforms are shown in Figure 2.12.

Example 3

An astable to switch a 12V, 160Ω relay on for 3 secs. and off for 2 secs.

Supply voltage 12V ± 1V. Ambient temperature 0 to +50°C.

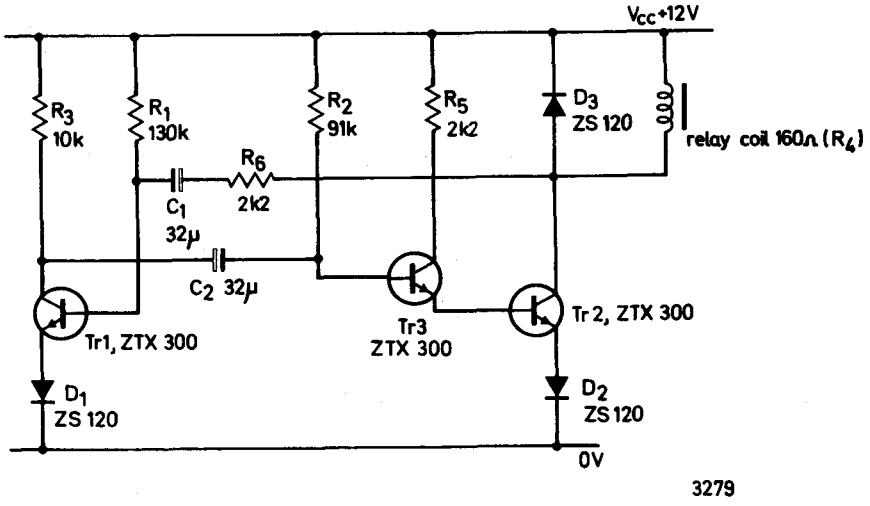


Figure 2.13. A low speed astable to switch a relay on for 3 seconds and off for 2 seconds.

Assume initially that a circuit similar to Figure 2.12 will be used with the relay coil replacing R4.

(1) With a 12V supply, protection diodes are required in the emitters of Tr1 and Tr2.

(2) Choose transistor type ZTX300, can switch required voltage and current.

(3) With 11V supply, assuming 20% tolerance on relay coil resistance:

maximum collector current of Tr2 $= \frac{11 - V_d - V_{ce(sat)}}{160} \times \frac{100}{80}$

(V_d = diode voltage). $= \frac{10}{160} \times \frac{100}{80} = 78\text{mA}.$

minimum current gain of ZTX300 at 78mA = 50 at 25°C.
= 41 at 0°C.

minimum base current required to saturate $= \frac{78}{41} = 1{\cdot}9\text{mA}$ with R2 20% high.

(4) Maximum value of R2 $= \frac{11 - V_d - V_{be}}{1{\cdot}9} \times \frac{100}{120}$ kΩ.
$= 4{\cdot}1\text{k}\Omega$ nominal.

(5) For the Tr2 to be turned off for 2 seconds CR $= \frac{2}{0{\cdot}7} = 2{\cdot}86$ secs.

If R2 = 3·9k then C2 = 730μF. This value is not impracticable but it is inconveniently high. A lower value can be used if Tr2 is replaced by a Darlington pair as shown in Figure 2.13.

(6) Referring to (3) above. Tr3 emitter current = 1·9mA.
Minimum current gain of ZTX300 at 1·9mA = 35 at 25°C.
= 29 at 0°C.

Minimum base current required to saturate Tr3 with R2 20% high $= \frac{1{\cdot}9}{29} = 65\mu\text{A}.$

(7) Maximum value of R2 $= \frac{11 - V_d - V_{be2} - V_{be3}}{65\mu\text{A}} \times \frac{100}{120}$
$= \frac{8{\cdot}6}{65} \times \frac{100}{120}$ MΩ $= 110\text{k}\Omega.$

If a value of 91kΩ is chosen for R2 then a close approximation to the required time constant is obtained if C2 = 32μF. R5 is chosen merely to limit the collector current of Tr3 to a safe value in excess of 1·9mA. 2k2 is suitable.

(continued overleaf)

(8) From equation 2.3 $R1C1 > 5{\cdot}8\ R3C2$.

but $R1C1 = \frac{3}{2}\ R2C2$ since Tr1 is off for 3 secs.

hence $R2C2 > 3{\cdot}9\ R3C2$

i.e. $R3 < \frac{R2}{3{\cdot}9} = \frac{91k}{3{\cdot}9} = 23{\cdot}3k\Omega$.

This is the maximum value that may be used. In this design R3 = 10kΩ will be used.

(9) Maximum collector current of Tr1 $= \frac{11 - V_d - V_{ce(sat)}}{10k} \times \frac{100}{80}$

$= 1{\cdot}25mA.$

minimum current gain of ZTX300 at 1·25mA = 27 at 0°C.

minimum base current to saturate Tr1,

with R1 20% high. $= \frac{1{\cdot}25}{27} = 46{\cdot}3\mu A.$

(10) Maximum value of $R1 = \frac{11 - V_d - V_{be1}}{46{\cdot}3} \times \frac{100}{120}\ M\Omega.$

$= 170k\Omega.$

(11) If R1 is made 130kΩ a close approximation to the required time constant of $\frac{3}{0{\cdot}7}$ seconds is obtained with C1 = 32μF.

The finished circuit is shown in Figure 2.13. It was found necessary to include R6, to prevent spurious operation due to inductive ringing in the relay coil, but it has virtually no effect on the timing. Diode D3 protects Tr2 from the inductive spike produced when Tr2 turns off.

Example 4

A wide range astable for generating repetitive pulses.

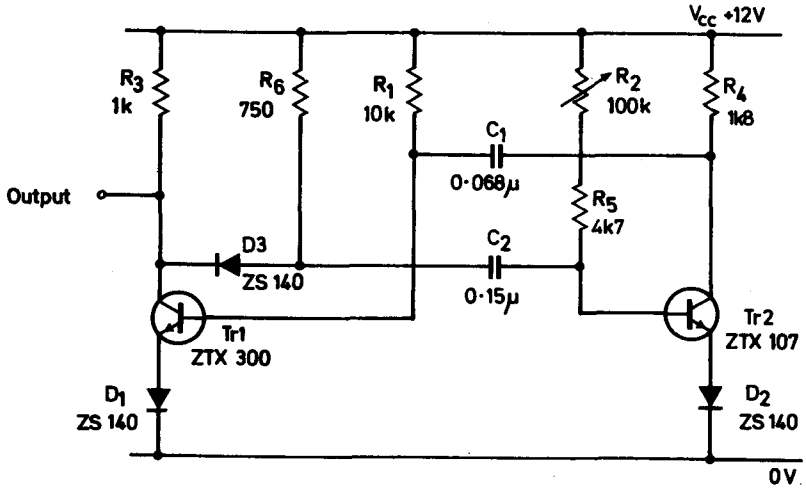


Figure 2.14. A variable speed astable with a 10 : 1 range.

No design procedure will be given for this circuit as it is basically the same as example 2, but the design is complicated by the need for the duration of one of the quasi-stable states to be variable over a wide range. A high gain transistor is essential for Tr2 and type ZTX107 was chosen.

With the component values shown T1 (= 0·7C1 . R1) is constant at 0·5mS but T2, defined by (R2 + R5), is variable over a range of 0·5 to 10·5mS. This gives a range of repetition time of 1mS to 11mS. Other time ranges can be accommodated by the choice of suitable capacitor values. A table is given below.

The output waveform at Tr1 collector is a rectangular pulse with rise and fall times of less than 50nS.

C1	C2	p.r.f.
680pF	1500pF	10μS to 110μS
6800pF	0·015μF	100μS to 1·1mS
0·068μF	0·15μF	1mS to 11mS
0·68μF	1·5μF	10ms to 110mS

SECTION 3

MONOSTABLE MULTIVIBRATORS

A monostable (Figure 3.1) has one a.c. coupling and one d.c. coupling. This gives it one stable state in which it normally rests and a quasi-stable state into which it can be triggered by means of an external pulse.

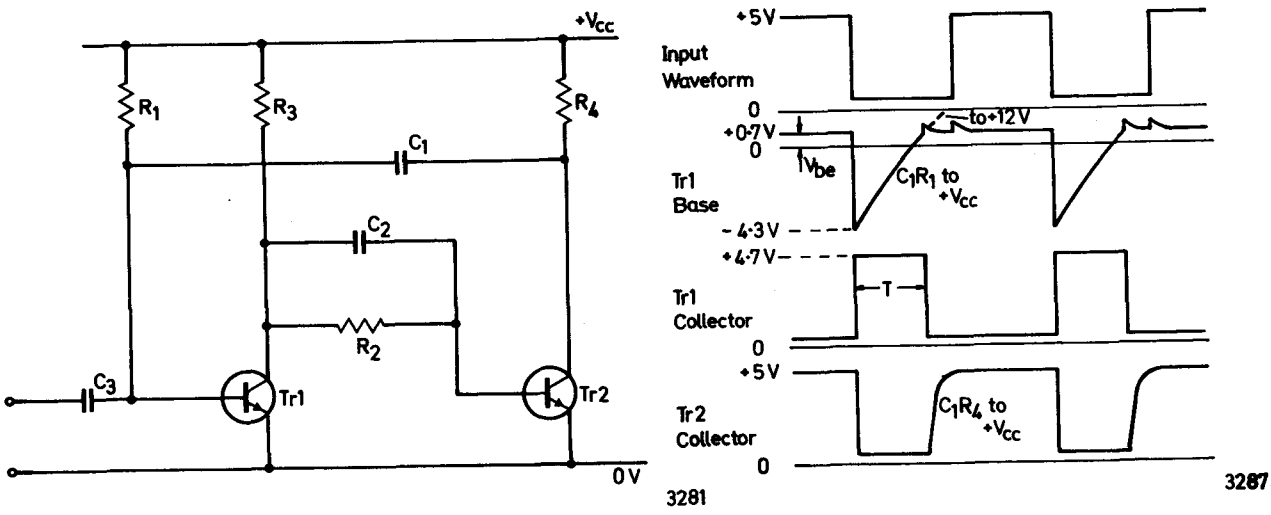


Figure 3.1. Basic Monostable, with waveforms.

Typical component values: R1 = R2 = 15kΩ
R3 = R4 = 1kΩ
C1 = 0·1μF
C2 = 100pF
C3 = 150pF (minimum)
Tr1 = Tr2 = ZTX300

Pulse width, T = 1mS, V_{cc} = +5V.

The timing equations for the circuit shown in Figure 3.1 are similar to those for the basic astable, the duration of the quasi-stable state being given by T = 0·7C1R1. Capacitor C2 is a "speed up" capacitor which reduces the turn-off time of Tr2 by rapidly removing the stored charge. It does not normally influence the timing.

This circuit is triggered from the negative edge of the input waveform and C3 must be as small as possible so that it does not influence the timing. Generally C3 < 0·1 C1.

In some cases when the positive edge of the input waveform occurs before the end of the quasi-stable state the circuit may re-set prematurely. This can be prevented by the addition of a diode and a resistor as shown in Figure 3.2.

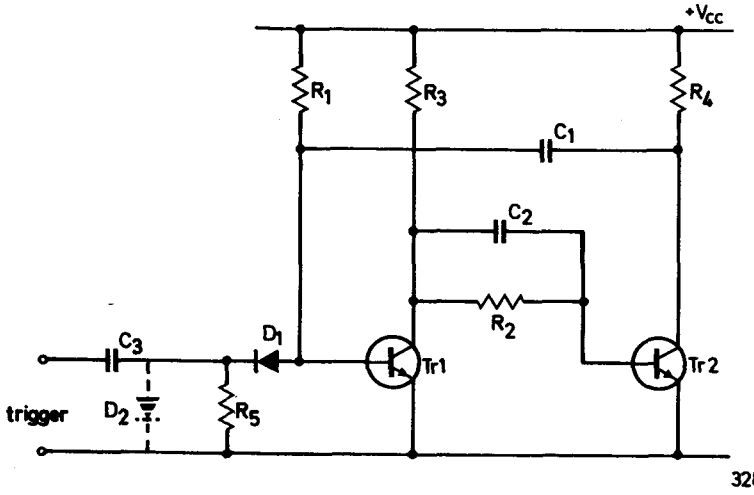


Figure 3.2. Negative Trigger Monostable.

Typical component values as Figure 3.1 except:

R5 = 15kΩ
D1 = ZS140
D2 = ZS140 (if required)

Figure 3.3. Positive Trigger Monostable.

Typical component values as Figure 3.1 except:

R5 = 15kΩ
D1 = ZS140
D2 = ZS140 (if required)

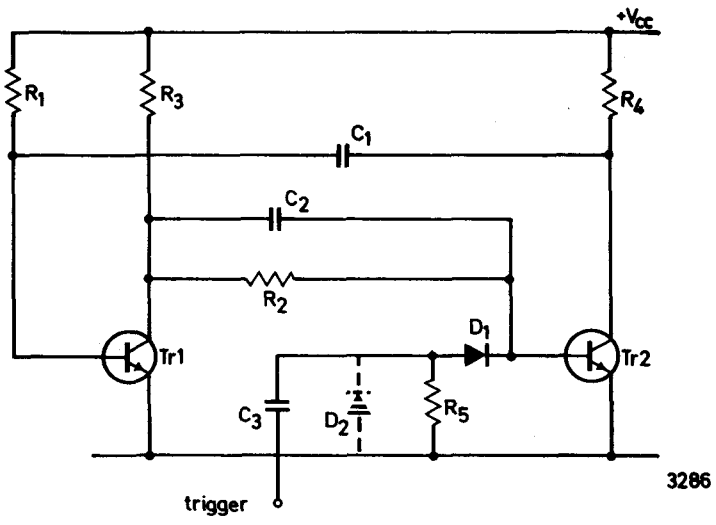


Figure 3.3 is a modification of Figure 3.2 to enable the circuit to trigger on the positive edge of the input waveform. To ensure that the trigger capacitor recharges fully between trigger pulses the time constant C3R5 should be much less than the duration of the positive part of the trigger waveform for Figure 3.2, and the negative part of the trigger waveform for Figure 3.3 It is usually convenient to make R5 about the same value as R1 or R3 although higher values can be used in low speed circuits. For high speed operation a diode can be connected across R5 as shown.

An alternative method of triggering from the positive edge of the input waveform is shown in Figure 3.4. In this circuit the values of R5 and C3 should be chosen so that the duration of the trigger pulse at Tr3 collector is much shorter than the required pulse.

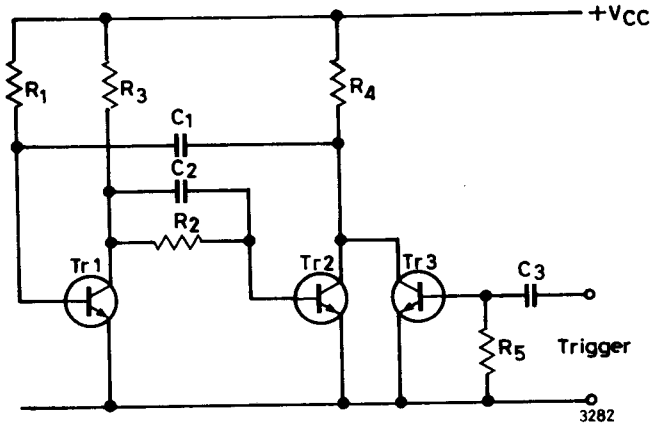


Figure 3.4. Transistor Triggered monostable.

Typical values as Figure 3.1 except:

R5 = 15kΩ
C3 = 100pF
Tr3 = ZTX300

At low speeds the values of C2 and C3 can be 10-1000 times less than C1. At high speeds the minimum values should be determined experimentally using high gain transistors. The graphs given in Section 1 will give the approximate values required and these should be regarded as minimum.

With supply voltages greater than 5V protection diodes are necessary for Tr1, as discussed in Section 2. Also the output waveform from Tr2 has a slow positive edge due to the need for C1 to re-charge through R4. This can be overcome by the addition of a diode and a resistor as discussed in Section 2. p-n-p transistors can be used in all the circuits if the supply voltage and all diodes are reversed. All the waveforms produced will also be inverted.

Simple Monostable

For non-critical applications where the required pulse is shorter than the input pulse and high accuracy is not required, the simplified circuit shown in Figure 3.5 may be used. C1 and R1 are the timing components and the pulse width produced depends on the amplitude of the input signal. The input should not exceed 5V pk-pk. If the input signal amplitude is equal to the supply voltage $T = 0{\cdot}7\,C1R1$.

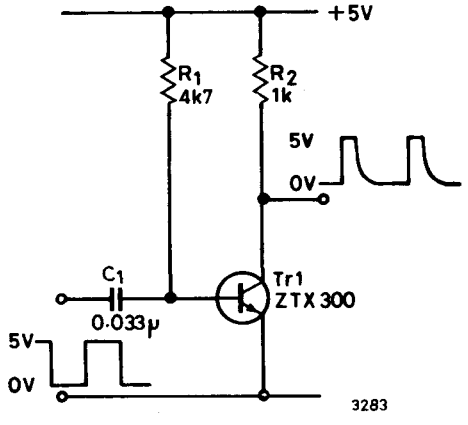


Figure 3.5. Simple Monostable for non-critical applications.

With component values shown, T = 100μS.

Emitter-coupled Monostable (Figure 3.6)

This is a "current mode" circuit, in which the transistors do not saturate. Under quiescent conditions Tr1 is cut off and Tr2 is fully conducting. Tr3 is a constant current source. The input pulse is differentiated by C2 and R2 and on the positive edge diode D1 conducts and forward biases the base of Tr1. Tr1 starts to conduct, its collector voltage drops and this change is coupled via Tr2 and C1 back to the emitter of Tr1, causing a further increase in current. This regenerative action ends with Tr2 cut-off and Tr1 conducting all the current provided by Tr3. During the quasi-stable state C1 discharges linearly, with current defined by Tr3, until the emitter voltage of Tr2 falls to a level where Tr2 starts to conduct. The current flowing in Tr1 falls, its collector voltage rises and the circuit rapidly switches back to its original state, charging C1 through Tr2, D2 and R4. The pulse width can be estimated as follows:

current provided by Tr3 = 5·3mA.

voltage swing across R1 = IR1 = 5·3 × 750 = 4 volts. However C1 only has to charge through 2·6 volts due to the "step" produced by the V_{be} of Tr1 and the forward voltage of D2.

i.e. C1 charging voltage = I . R1 − V_{be1} − V_{d2}.

$$IT = CV \text{ therefore } T = \frac{2000 \times 10^{-12} \times 2{\cdot}6}{5{\cdot}3 \times 10^{-3}} \text{ seconds}$$

$$= 0{\cdot}98\mu S \text{ with component values given.}$$

Other pulse widths may be obtained by choice of a suitable capacitor. Figure 3.6 shows the actual output waveform obtained, with a measured pulse width of just over 1μS.

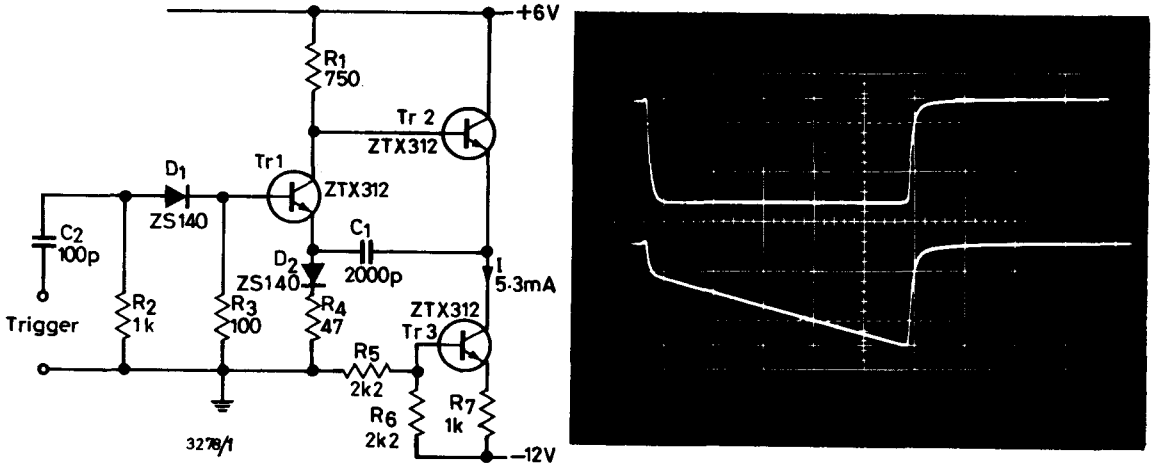


Figure 3.6. Emitter Coupled Monostable, with waveforms.

With component values shown, pulse width T = 1μS.

Rise and fall times are less than 20nS.

Upper trace	—	Tr1 collector
Lower trace	—	Tr2 emitter
Vertical scale	—	2V/cm
Horizontal scale	—	200nS/cm

Trigger—4V pk.-pk. minimum. Rise time = 10nS.

Design Examples

Example 1

A general purpose monostable to operate from a 5V ±10% supply, with an output impedance of 1kΩ. Resistor tolerance 10% nominal, 20% end of life. Temperature −10°C to +50°C.

Circuit—Refer to Figure 3.1

(1) Choose suitable transistor. ZTX300.

(2) Choose collector load resistors R3, R4. 1kΩ nominal.

(3) Minimum supply voltage and minimum temperature are the worst conditions for turning the transistor fully on. With 4·5V d.c. supply, collector current of Tr1 and Tr2 = 4·5mA nominal.
=5·6 mA maximum.

(4) Minimum current gain of ZTX300 at 5·6mA = 45 at 25°C.
= 34 at −10°C.
Hence the minimum base current to saturate $= \frac{5{\cdot}6}{34} = 0{\cdot}165\text{mA}$.

(5) Maximum base circuit resistance $= \frac{4{\cdot}5}{0{\cdot}165} \times \frac{100\text{k}\Omega}{120} = 18{\cdot}7\text{k}\Omega$.

i.e. R1 max. = 18·7kΩ and R2 max. = 17·7kΩ since R3 is in series with R2.

15kΩ was chosen for both R1 and R2 as with this value the pulse width produced is numerically similar to the value of C1; i.e. 0·1μF gives 1mS.

(6) The worst condition for triggering in Tr1 is that R1 should be at the low end of its tolerance and R3 should be high. Under these conditions with 5·5V supply,

Tr1 base current = 400μA.

Tr1 collector current = 4·6mA, i.e. $\frac{I_c}{I_b} \approx 10$.

Putting these figures into the trigger charge g aph, Figure 1.5 gives a trigger charge of 560 pico-coulombs. If we assume that the trigger voltage is 4 volts then:

$$C3 = \frac{560}{4} = 140\text{pF}.$$

The nearest preferred value above this is 150pF and this indicates a minimum value of 1500pF for C1 giving a minimum pulse width of 15μS. Shorter pulses can be obtained with reduced accuracy.

(7) Similarly for Tr2 but using the "stored charge" graph of Figure 1.3. Stored charge = 390 pico-coulombs. With a 5·5 volt supply the voltage swing on Tr1 collector is approximately 5 volts. Hence $C2 = \frac{390}{5} = 78\text{pF}$ minimum.

A value of 100pF was chosen for C2.

The finished circuit is shown in Figure 3.1. If ZTX311 transistors are used instead of ZTX300, C3 can be reduced to 10pF and C2 to 5pF minimum giving a minimum pulse width of 1μS, with C1 = 100pF.

Example 2

A high speed monostable with pulse width variable over a 4 : 1 range, down to 100nS. Temperature 0°C to +50°C.

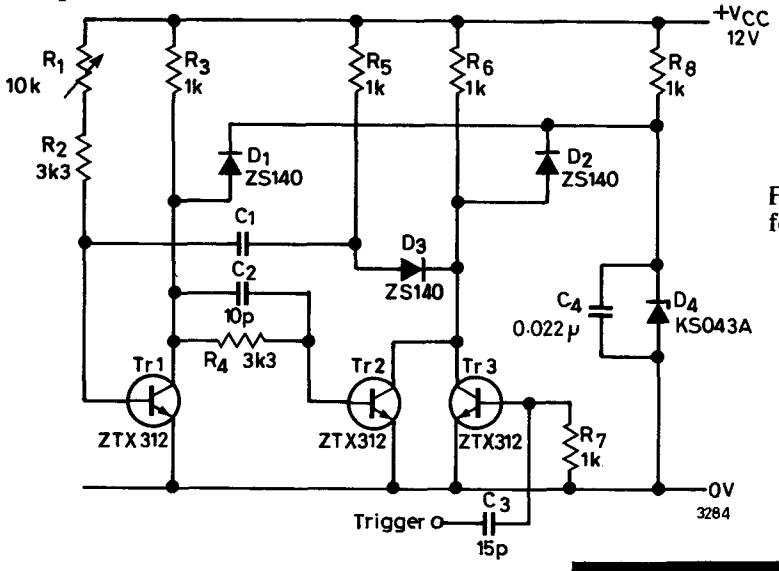
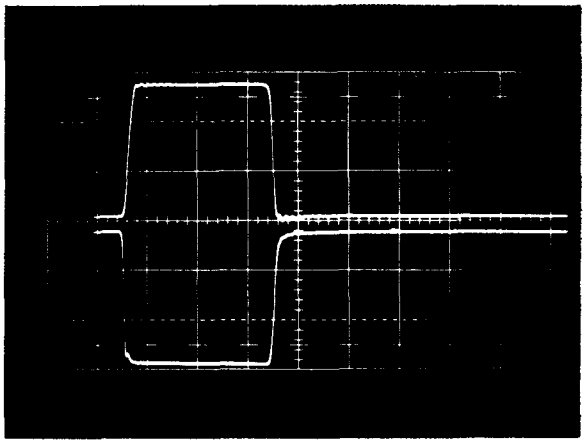


Figure 3.7.

Fast monostable and output waveforms, with C1 = 68pF.



Upper trace — Tr1 collector
Lower trace — Tr2/Tr3 collectors
Vertical scale — 2V/cm
Horivontal scale — 100nS/cm

(1) To achieve maximum speed it is desirable that a low value of load resistor should be used and the transistors should be operated close to the peaks of their h_{FE}/I_c and f_T/I_c curves.

With ZTX312 devices this occurs in the 10-20mA region. To obtain the best possible waveform a 12V supply is used with catching diodes limiting the collector voltage to 5 volts and an isolating diode (D3) is used to provide a separate recharge path for the timing capacitor C1. Choosing a value of 1kΩ for R5, R6.

nominal collector current of Tr2 $= \frac{12}{500\Omega} = 24\text{mA}.$

maximum collector current of Tr2 $= 24 \times \frac{100}{80} = 30\text{mA}.$

minimum current gain of Tr2 at this current = 35 at 25°C.
= 29 at 0°C.

hence minimum base current to saturate $= \frac{30}{29} = 1{\cdot}03\text{mA}.$

(2) Nominal base current $= 1{\cdot}03 \times \frac{120}{100} = 1{\cdot}24\text{mA}.$

Tr2 collector is caught at + 5 volts, therefore the maximum value of R4 $= \frac{5 - 0{\cdot}85}{1{\cdot}24} = 3{\cdot}35\text{k}\Omega$
i.e. R4 = 3·3kΩ nominal.

(3) A value of 1kΩ was chosen for R3 to provide adequate drive to Tr2 and to allow Tr1 to operate close to the peaks of its h_{FE}/I_c and f_T/I_c curves.

maximum current required from Tr1 $= \frac{12}{1\text{k}} \times \frac{100}{80} = 15\text{mA}.$

(continued overleaf)

(4) Current gain of Tr1 at 15mA = 40 at 25°C.
= 33 at 0°C.

minimum base current for saturation $= \frac{15}{33} = 455\mu A.$

maximum base resistance $R1+R2 = \frac{(12-0{\cdot}85)}{0{\cdot}455} \times \frac{100}{120}$ kΩ.

$= 20{\cdot}4k\Omega.$

A lower value than this can be used and in order to obtain a 4 : 1 range R1 was made 10kΩ and R2 = 3·3kΩ. This completes the d.c. design.

(5) With R5 and R6 high, and R4 low:

collector current of Tr2 = 20mA.

base current of Tr2 = 1·9mA, i.e. $\frac{I_c}{I_b} \approx 10.$

Referring to the "stored charge" graph, Figure 1.3, the stored charge under these conditions is 50 pico-coulombs. With a 5V swing on Tr1 collector the minimum value of C2 $= \frac{50}{5}$ = 10pF.

(6) Transistor triggering was chosen since this gives high trigger sensitivity with good isolation between the timing circuit and the trigger source. R7 was chosen empirically as 1kΩ and C3 increased until reliable triggering was obtained under all conditions, with a 4V pk-pk trigger signal. This occurred with C3 = 10pF and a value of 15pF has been chosen for the final circuit to allow for component spreads. As R7C3 = 15nS the trigger pulse is much shorter than the minimum pulse width required and will not affect the timing.

(7) C1 is chosen according to the pulse width required, the timing equation is T = 0·38C1 (R1+R2). The output waveforms with C = 68pF and R1 adjusted for a pulse width of 300nS is shown in Figure 3.7. Rise and fall times are about 10nS. Figure 3.8 shows the trigger pulse at Tr2 collector with C1 removed.

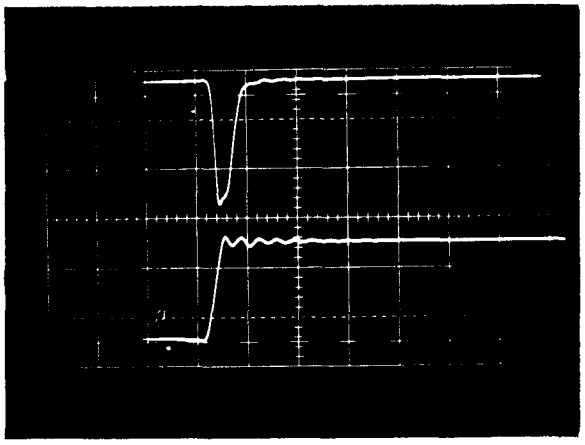


Figure 3.8. Trigger pulse at Tr2/Tr3 collectors, with C1 disconnected.

Upper trace	—	Tr2/Tr3 collectors
Lower trace	—	Trigger waveform
Horizontal scale	—	50nS/cm
Vertical scale	—	2V/cm

SECTION 4

BISTABLES AND COUNTERS

If we replace the two a.c. couplings of the basic astable with two d.c. couplings, we get a bistable (Figure 4.1). This circuit has two stable states and will remain in either until triggered into the opposite state by an external pulse. Bistables have many applications including counters, shift registers and memory elements, but in most cases it is more economical to use integrated circuits than discrete components. The exceptions are (a) when the supply voltages or the input and output requirements are incompatible with I.C.'s; (b) when very low power dissipation is required; (c) when very low or very high speed operation is required and (d) when only a very simple counting circuit is required (e.g. organ dividers).

Counting bistables are the most suitable for discrete components and only this type will be described.

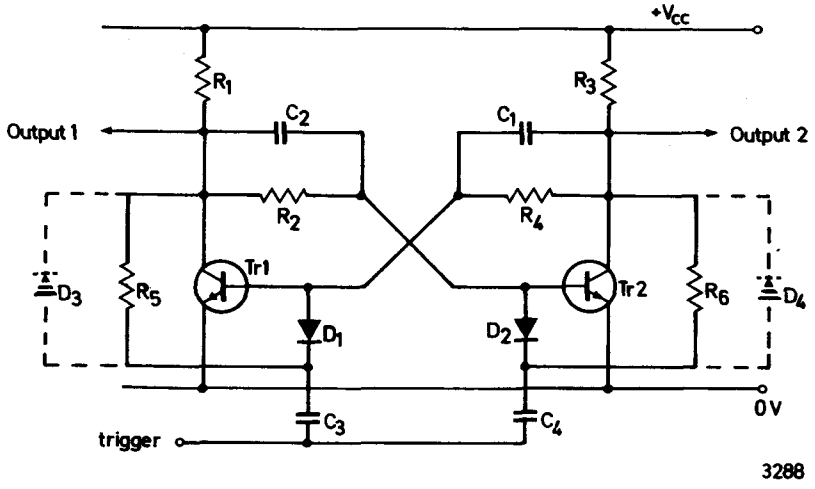


Figure 4.1

Typical component values:

R1	=	R3	=	1kΩ
R2	=	R4	=	10kΩ
R5	=	R6	=	10kΩ
C1	=	C2	=	220pF
C3	=	C4	=	470pF
D1	=	D2	=	ZS140
D3	=	D4	=	ZS140
Tr1	=	Tr2	=	ZTX300
$+V_{cc}$	=	5V		

Note: Without D3, D4 maximum trigger rate = 200kHz
With D3, D4 maximum trigger rate = 400kHz

Assume that initially Tr1 is saturated and Tr2 is cut off. Under these conditions diode D2 is reverse biased by slightly less than V_{cc} but diode D1 has a small forward bias. The trigger pulse is differentiated by C3R5 and C4R6 and on the negative edge D1 conducts and reverse biases Tr1. As Tr1 starts to turn off its collector voltage rises, Tr2 starts to conduct and its collector voltage falls reducing the base current of Tr1. The regenerative action ends with Tr2 saturated and Tr1 cut off. The bias on the "steering" diodes D1 and D2 is now reversed so that the negative trigger pulse cuts off Tr2 and the circuit reverts to its original state. Diodes D3 and D4 can be added if desired to reduce the recharge time of the trigger capacitors, for high speed operation.

The method of triggering shown in Figure 4.1 is the most popular and generally the most satisfactory, but there are other methods.

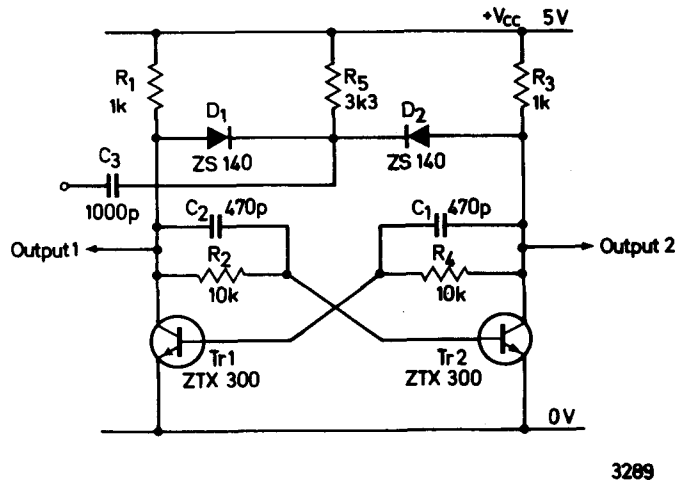


Figure 4.2. An example of collector triggering. Maximum trigger rate = 100kHz.

Figure 4.2 shows an example of collector triggering. Assuming that Tr1 is saturated and Tr2 is cut off, diode D1 will be reverse biased by 5V and diode D2 by about 0·5V. The trigger waveform is differentiated by C3 and R5, and on the negative edge, diode D2 conducts pulling down the collector voltage of Tr2. This transient change is coupled via C1 to the base of Tr1, causing Tr1 to turn off. As Tr1 collector voltage rises Tr2 turns on, its collector voltage falls further, and the circuit switches.

Because C1 and C2 have to act as a transient memory their value needs to be greater than would be suggested by charge storage considerations. 470pF is the minimum for ZTX300 devices in the circuit shown, but higher values may be used. Problems sometimes arise with this circuit when several stages are cascaded since there is no isolation between the trigger and the output. Maximum trigger rate = 100kHz.

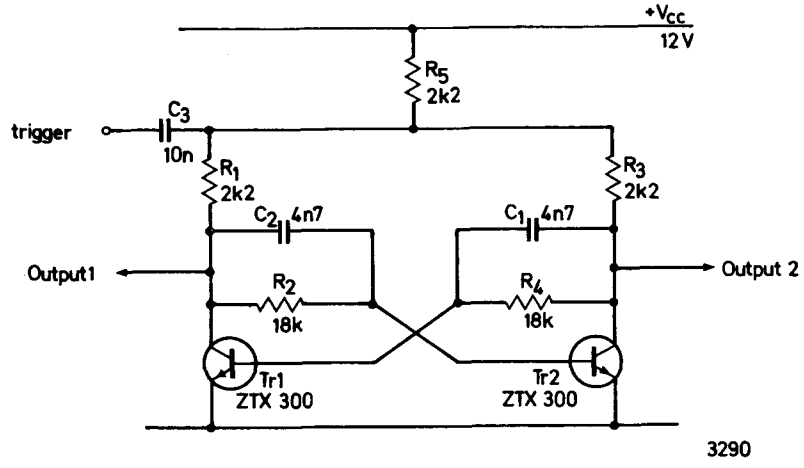


Figure 4.3. A simple method of collector triggering for low speed bistables (e.g. organ dividers).

With component values shown, the circuit will operate at trigger rates up to 50kHz, but output waveform is poor above 20kHz.

Figure 4.3 shows a very simple method of triggering, suitable for low speed bistables. The trigger waveform is differentiated by C3 and R5. If Tr1 is saturated and Tr2 is cut off then nothing appears on Tr1 collector but the differentiated trigger waveform appears on the collector of Tr2. The negative edge is coupled via C1 to the base of Tr1 and momentarily turns it off. As Tr1 collector voltage rises Tr2 starts to turn on and rapidly turns off Tr1. The state of the circuit reverses again at the next negative trigger pulse.

The capacitor values shown in Figure 4.3 are the minimum for the component values used and this circuit will operate at trigger rates of up to 50kHz. For lower speed operation larger values of capacitances are desirable but a ratio of 2 : 1 should be kept between C3 and C1, C2.

Determining the minimum values of trigger and speed-up capacitors

Taking the circuit shown in Figure 4.1 as an example, the minimum value of speed-up capacitance can be determined as follows; assuming 20% of life resistor tolerance and 10% supply voltage tolerance:—

minimum collector current with 5·5V supply $= \frac{5{\cdot}5}{1k} \times \frac{100}{120} = 4{\cdot}6mA.$

maximum base current with 5·5V supply $= \frac{(5{\cdot}5 - 0{\cdot}7)}{11k} \times \frac{100}{80} = 0{\cdot}55mA.$

i.e. $\frac{I_c}{I_b} = 8{\cdot}4.$

From the "speed up" charge graph, Figure 1.3, the stored charge of a ZTX300 under these conditions is approximately 550pC. Assuming a collector voltage swing of 5V pk-pk the minimum speed-up capacitance is 110pF.

Putting the above figures into the "trigger charge" graph, Figure 1.5 indicates a minimum trigger charge of about 700pC, i.e. 175pF minimum with a 4V pk-pk minimum trigger signal. However, a slightly higher value than this is required in practice because some of the trigger charge is lost in the steering diodes D1 and D2, and the steering resistors R5 and R6. The true value may be determined with the circuit shown in Figure 4.4 which is in effect half of the bistable built with worst case component values to ensure that the transistor is heavily saturated.

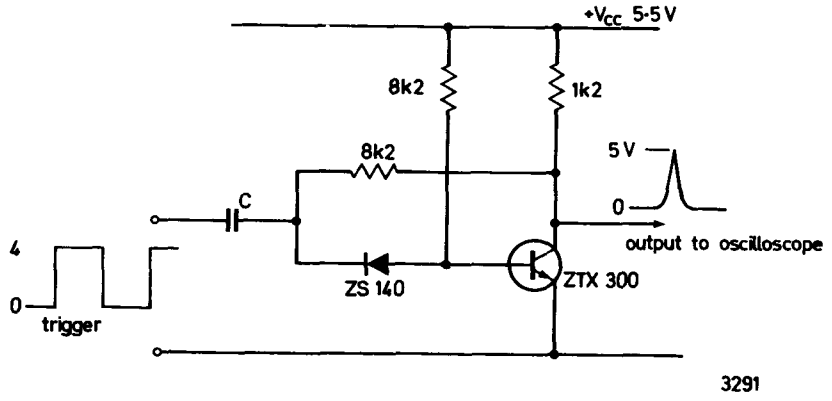


Figure 4.4. Test circuit for determining the minimum value of trigger capacitance needed for the circuit shown in Figure 4.1. "C" is increased until an output pulse of 5V minimum amplitude is obtained with all samples of transistor ZTX300.

It was found that the minimum value of "C" to fully turn off all samples of ZTX300 was 220pF.

To ensure reliable operation larger values of capacitance have been used in the final circuit, the speed-up capacitors being 220pF and the trigger capacitors 470pF. The d.c. design for this bistable follows the same lines as for astables and monostables and will not be described here.

Binary Counters

Any number of bistables may be connected in cascade, the count being 2^n where n is the number of stages. When division ratios that are not a power of 2 are required, feed-back, feed-forward and gating can be used to obtain the required count.

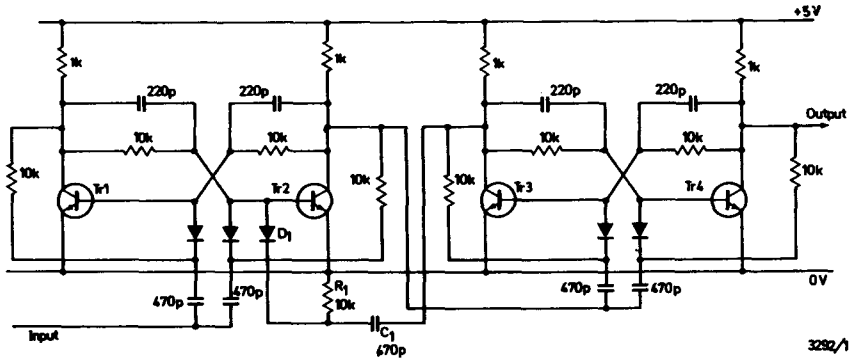
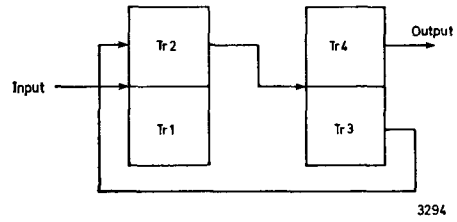


Figure 4.5. Two-stage binary counter with feedback to reduce the count to 3.

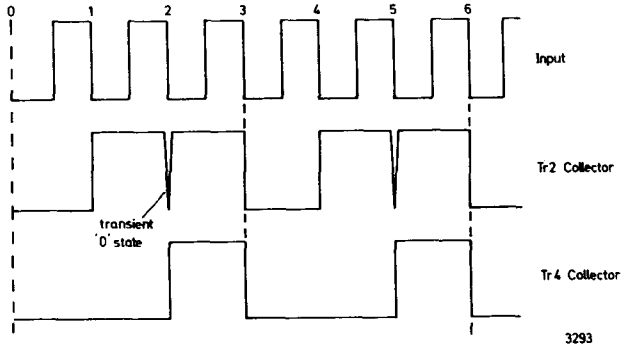
All transistors — ZTX300
All diodes — ZS140

Pulse No.	Tr2	Tr4
0	0	0
1	1	0
2	0 transient state	1
2	1	1
3	0	0

0 = low (0·2V), 1 = high (4·5V)



Schematic



Waveforms

Figure 4.5 shows a two-stage counter modified to give a count of 3 by means of feed-back from Tr3 to Tr2. Assuming that Tr2 and Tr4 are initially in the "0" state (conducting with V_{ce} = 0·2V) the first input pulse triggers Tr2 into the "1" state. The second input pulse returns Tr2 to the "0" state which in turn triggers Tr4 into the "1" state. Tr3 meanwhile goes to "0" and triggers Tr2 back into the "1" state (all this happens in less than 1μS). The third input pulse returns Tr2 to the "0" state, which in turn returns Tr2 to the "0" state, and the circuit reverts to its starting point.

Feed-back from the last to the first stage of a 3-stage binary counter would give a count of 7 instead of 8, to the second stage would give a count of 6 (2 × 3) and to both the first and second stages would give a count of 5. In general feed-back to the first stage of a counter will reduce the count by 1 to the second stage by 2, to the third stage by 4, etc., any combination being possible. This technique is quite satisfactory for simple frequency dividers and counters but where all the outputs are used care should be taken to see that the transient "0" states produced do not interfere with other circuitry.

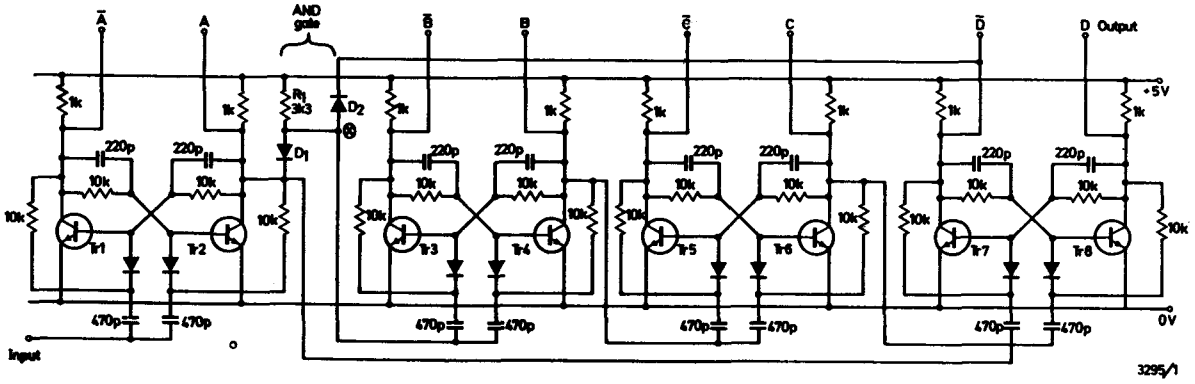
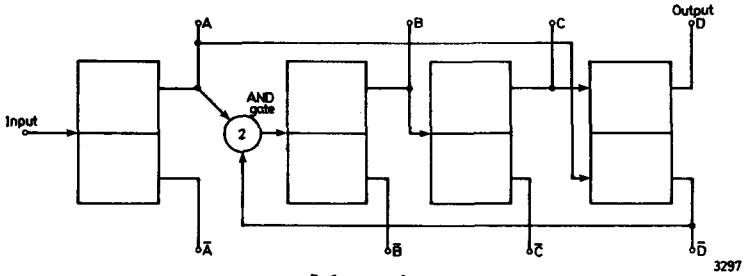


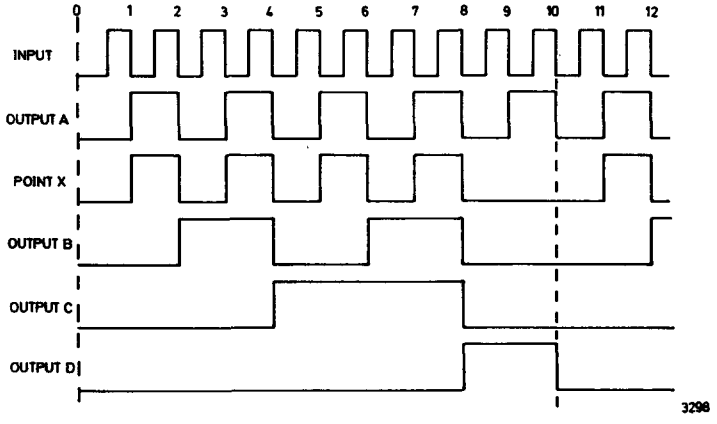
Figure 4.6. Decade counter using four bistables, with an AND gate between the first and second stages and feed forward from the first stage to reset the fourth.

All transistors — ZTX300
All diodes — ZS140

Pulse No.	D	C	B	A	X
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	0
10	0	0	0	0	0



Schematic



Waveforms

Figure 4.6 shows a decade counter, using gating between the first and second stages and feed-forward from the first to the fourth stage. Up to the 8th pulse the AND gate is open and the circuit operates as a simple binary counter. On the 8th pulse Tr8 is triggered from the "0" state to the "1" state whilst Tr7 goes to "0" closing the AND gate.

The 9th pulse triggers Tr2 into the "1" state and on the 10th pulse Tr2 goes to "0" and resets Tr7 to the "1" state and Tr8 to "0", the cycle then repeats. No transient states are produced by this circuit.

Ring Counters

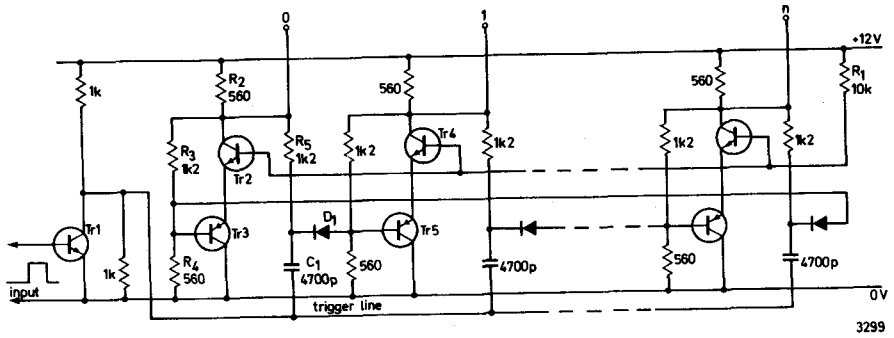
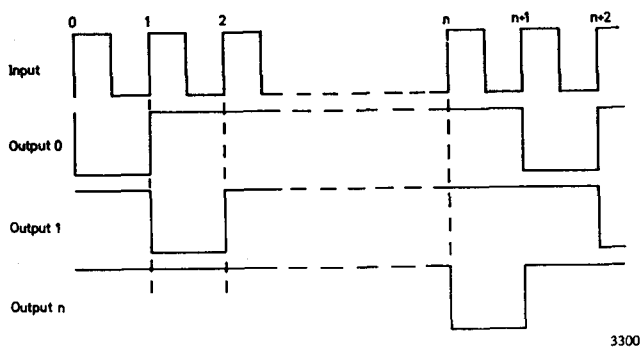


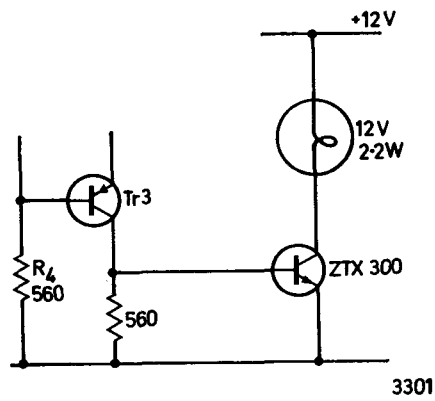
Figure 4.7. Practical ring counter circuit.

(All stages are identical and any number can be connected in cascade).

All n-p-n transistors ZTX300
All p-n-p transistors ZTX500
All diodes ZS140



Circuit Waveforms



Modification to obtain an output to drive a lamp or another counter.

Ring counters are useful when one requires a count that is not a power of 2, or when one requires a separate output for each number instead of binary coded output. Ring counters tend to become uneconomical at counts above 10-12.

Figure 4.7 shows a practical circuit. Each of the n-p-n/p-n-p pairs forms a bistable element although bistable action is only exhibited when two or more stages are connected together. Only one stage can conduct at any given time and the conducting stage takes all the base current provided by R1, and steers the trigger pulse to the next stage in the ring. Assume that the "0" stage is conducting and all other stages are cut off, Tr2 is saturated with about 1·5V on its collector and 2·2V on its base. The base voltage of Tr3 is about 0·5V. For all other stages the collector and base of the n-p-n will be at 9V and 2·2V respectively whilst the base of each p-n-p transistor will be at 2·7V, i.e. cut-off. Diode D1 is forward biased by about 1·2V and all other diodes are reverse biased by about 7V. The first negative trigger pulse drives the base of Tr5 negative, Tr5 starts to conduct and the collector voltage of Tr4 falls, causing regenerative action which ends with the "1" stage conducting and all other stages cut off. The process repeats at each trigger pulse.

Any number of stages may be connected in the ring. The output of the last stage is always fed back to the input of the first. A direct read-out of the state of the counter can be obtained if the collector load resistor R2 of each stage is replaced with a 6V, 40mA lamp in series with a 100Ω resistor. ZTX302 and ZTX502 transistors are preferred in this case. To drive a more powerful lamp or to obtain an output to drive another counter the output circuit shown may be used.

SECTION 5

DIGITAL DISPLAY CIRCUITS AND DIGITAL TO ANALOGUE CONVERTERS

It is frequently required to present a numerical display for such applications as digital voltmeters, frequency meters, summation metering, etc. The current trend is also to replace the moving coil instrument by digital readout. This may be achieved by a variety of indicators. The following circuits show a few of these with the associated driving components.

Nixie Driver Circuit

A Nixie indicator consists of a gas filled tube with 10 cold cathodes and a common anode. The cathodes are, in fact, digits from 0 to 9 and are stacked one upon the other. A digit is illuminated by lowering its cathode potential to earth, other cathodes being maintained at some high potential, typically 100V. A glow discharge is then initiated between the anode and the selected digit, other digits remaining dark. The anode supply is usually 200V or greater. Transistor drivers are used to select the appropriate digit.

When a transistor is off, it is not uncommon for it to be drawn into the breakdown region by the large anode voltage but the current is limited to a small value. This leakage current can cause an unwanted background glow or, at worst, permanent illumination of a digit. Driver transistors ZTX341/2 (BSV28/29) have breakdown voltages of 100V and 120V respectively, at which the background glow is negligible.

A typical decoder circuit is shown. This circuit accepts an 8-line logical input in 8-4-2-1 binary coded decimal and decodes it to obtain the decimal equivalent. The operation of the circuit makes use of the fact that, if the least significant digit is eliminated, pairs of odd and even numbers share the same logic. There are thus two stages of selection. The first stage decides into which of five pairs the required number falls and the second stage decides whether the number is odd or even. Only one output can satisfy both conditions. The simplification of logic which this technique permits allows the cost of the circuit to be reduced significantly.

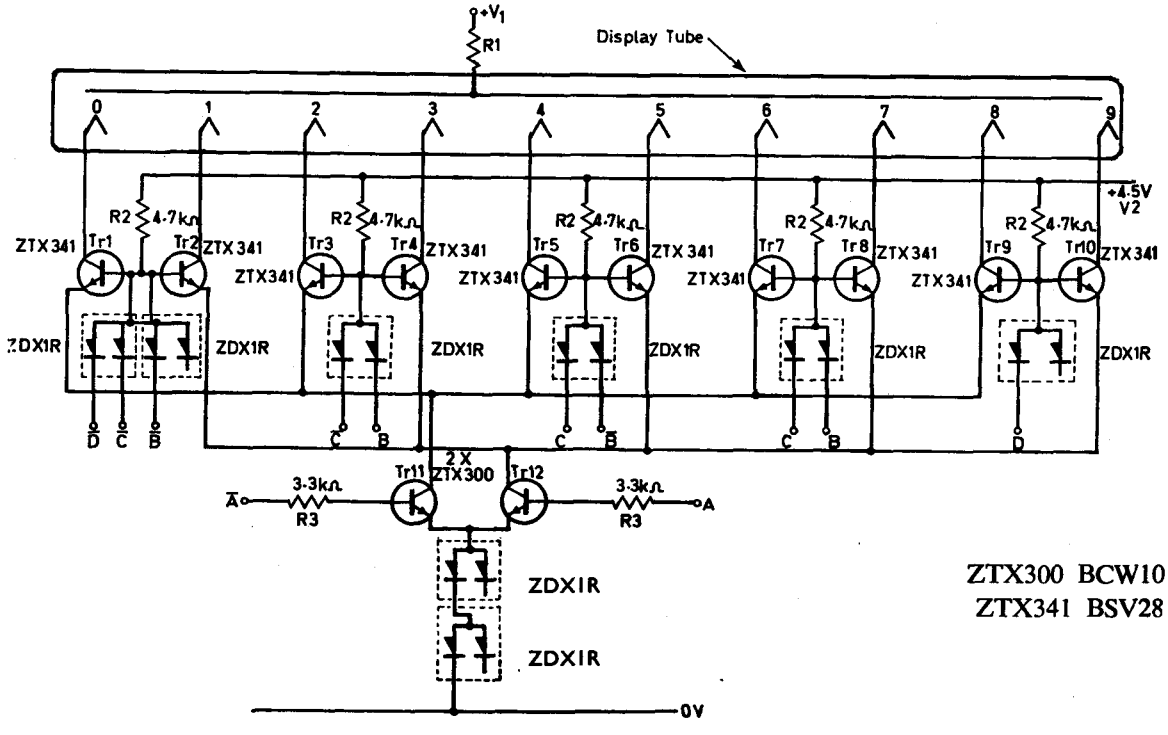


Figure 5.1

Decimal	Binary D C B	A	Logic (high = 1) positive notation
0	0 0 0	even 0	$\overline{D}\overline{C}\overline{B}$
1	0 0 0	odd 1	
2	0 0 1	0	$\overline{C}B$ $\overline{D}$ is redundant since the state 101 for DCB does not occur.
3	0 0 1	1	
4	0 1 0	0	$C\overline{B}$ $\overline{D}$ is redundant since the state 110 for DCB does not occur.
5	0 1 0	1	
6	0 1 1	0	CB $\overline{D}$ is redundant since the state 111 for DCB does not occur.
7	0 1 1	1	
8	1 0 0	0	D $\overline{C}\overline{B}$ is redundant since the states which would make C or B = 1 do not occur.
9	1 0 0	1	

Component Values

The values of the resistors used in this circuit depend upon the supply voltages available, the type of logic to be used and the current required by the display tube.

(R1) R1 is given by the relation $R1 = \frac{V1 - V_M}{I_K}$ kΩ

where V1 = high voltage supply available (200 to 350V).

V_M = display tube maintaining voltage, from manufacturer's data, (usually 140 to 170V).

I_K = recommended display tube cathode current, from manufacturer's data, (in mA).

As an example, for the popular 0·6" character height tube, the maintaining voltage is usually 140V and the cathode current 2mA, with a 340V supply; then

$$R1 = \frac{340 - 140}{2} = 100k\Omega$$

(R2) The table shows the value of R2 for different values of cathode current and supply voltage V_2. (Note supply voltage V_2 will normally be the same as the supply to the logic circuits used).

Supply Voltage V_2	Cathode Current		
	1-5mA	5-10mA	10-15mA
4-6V	3·3kΩ	1·5kΩ	1kΩ
10-14V	22kΩ	10kΩ	6·8kΩ
20-30V	47kΩ	22kΩ	15kΩ
25-35V	68kΩ	33kΩ	22kΩ

(R3) R3 is chosen such that there is sufficient input current to saturate Tr11 and Tr12 with the chosen value of cathode current.

Cathode Current	1-5mA	5-10mA	10-15mA
Input Current (min.)	0·2mA	0·4mA	0·6mA

In some cases it may be necessary to load the output of the logic counter stage driving Tr11 and Tr12 to ensure sufficient input current.

As an example, suppose that the circuit is to be driven from a Micronor 2 flip-flop (e.g. ZN322E/222E). The output of a Micronor 2 gate is equivalent to a diode in series with a resistor of 750Ω: so, with the minimum supply voltage of 4V and a temperature of 0°C this will be a voltage of 3·1V in series with 750Ω. The voltage required at the base of Tr11 and Tr12 will be approximately 2·4V.

$$\text{Therefore: } R3 = \frac{3{\cdot}1 - 2{\cdot}4}{0{\cdot}2}\,k\Omega - 750\Omega = 3{\cdot}5k\Omega - 750\Omega$$
$$= 2{\cdot}7k\Omega$$

for a cathode current of 1-5mA.

If, however, 15mA cathode current is required, the value of R3 approaches zero, and it is desirable to load the flip-flop output with 1kΩ resistors to supply additional current. In this case, the value of R3 is also 1kΩ.

The table shows the value of R3 required for the different values of cathode current considered.

Logic	Cathode Current		
0°C to 55°C	1-5mA	5-10mA	10-15mA
Micronor 2	2·7kΩ	1kΩ	1kΩ*
Series 54/74 TTL	2·2kΩ	1kΩ	1kΩ*

*1kΩ loading resistor.

Counter

The drawing shows a four-stage binary counter, using Micronor 2 elements, suitable for use with the Nixie driver circuit. Similar circuits can be built using TTL elements, high level logic or with discrete components as shown in Figure 4.6.

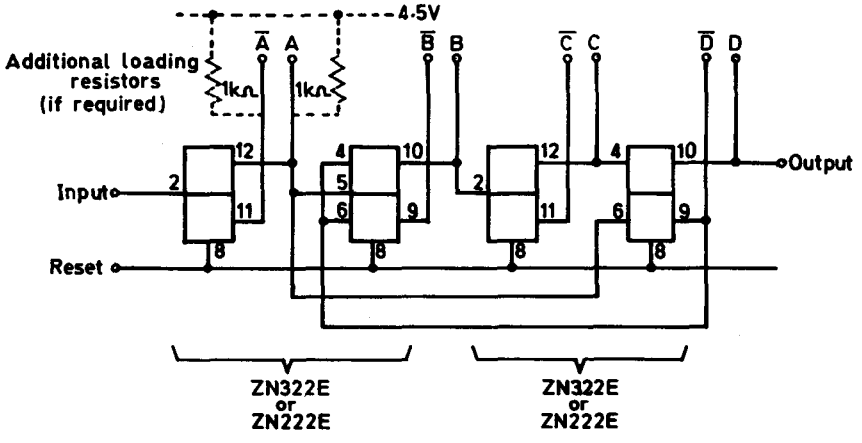
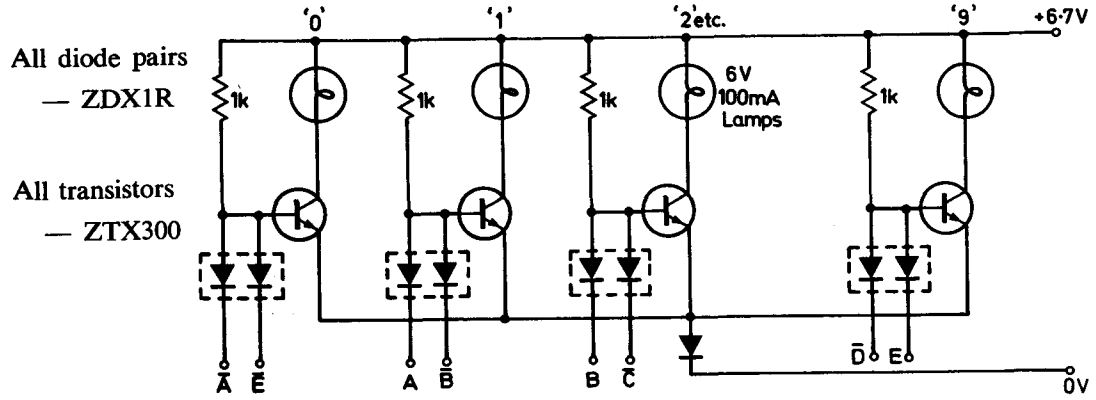


Figure 5.2

Projection and Edge Illumination Readout

This type of indicator uses incandescent lamps, usually ten per unit. The driving circuit must be able to energize any one of the lamps according to the logic states present at the input. A suitable circuit driven by a Johnson counter with ZN7474E D-type flip-flops, is shown in Figure 5.3. This type of counter requires only a simple two-input AND gate to give a unique output for each number, and ZDX1R diode pairs can be used to advantage. The common emitter-circuit diode provides a d.c. bias which holds off all except the selected transistor. Component values shown are suitable for lamps of 6V 100mA.



Pulse No.	Outputs A	B	C	D	E	Decoding logic
0	0	0	0	0	0	$\bar{A}.\bar{E}$
1	1	0	0	0	0	$A.\bar{B}$
2	1	1	0	0	0	$B.\bar{C}$
3	1	1	1	0	0	$C.\bar{D}$
4	1	1	1	1	0	$D.\bar{E}$
5	1	1	1	1	1	A.E
6	0	1	1	1	1	$\bar{A}.B$
7	0	0	1	1	1	$\bar{B}.C$
8	0	0	0	1	1	$\bar{C}.D$
9	0	0	0	0	1	$\bar{D}.E$

Positive logic, 1 = high
0 = low

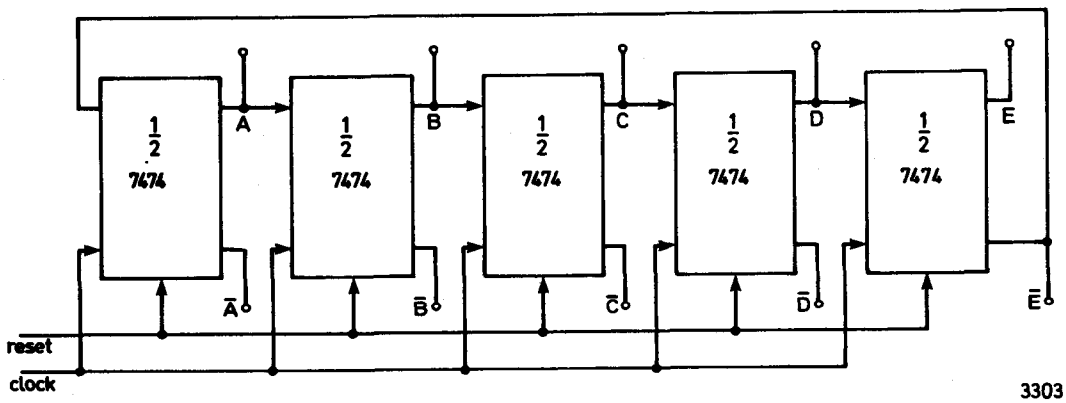


Figure 5.3. Filament lamp readout using ZDX1R diode pairs and ZN7474E D-type flip-flops in a Johnson decade counter.

4-Bit Digital-to-Analogue Converter

This circuit illustrates the use of complementary transistors as switches. Driver transistors are used, operating from supply rails greater than the switch supply rails to ensure that the switching transistors will bottom satisfactorily. A ladder network, consisting of suitable close tolerance resistors, is used to sum the components.

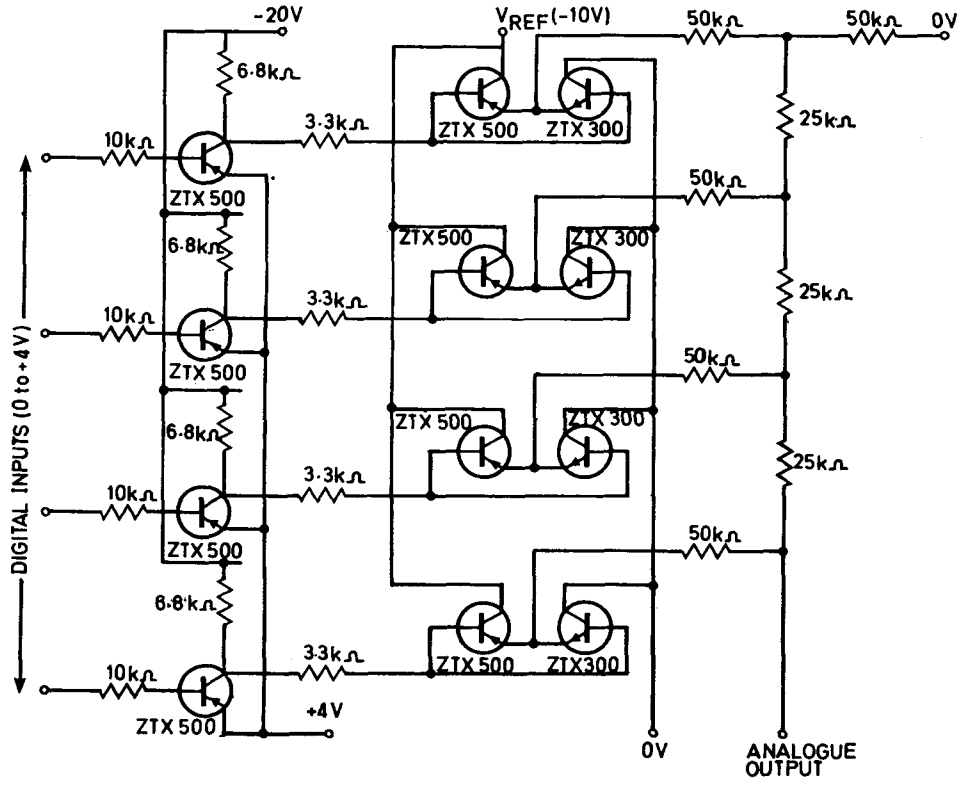


Figure 5.4

SECTION 6

RAMP AND STAIRCASE GENERATORS
PULSE COUNTERS

When a capacitor C is charged from towards a voltage V with a resistor R, the voltage rises exponentially according to the formula $v = V\left[(I-e^{-\frac{t}{CR}}\right]$ where v = instantaneous voltage t = time

In most ramp generator applications a linear charge is required and various methods of overcoming the non-linearity of the R-C circuit have been devised.

Constant Current Charge

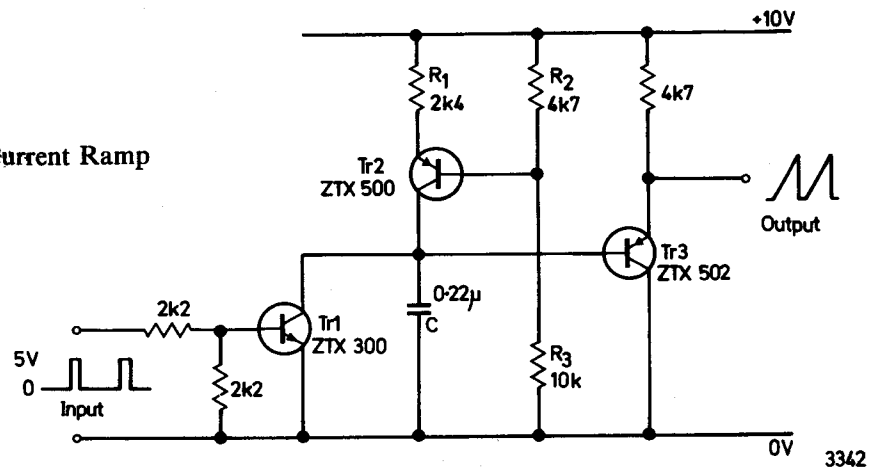
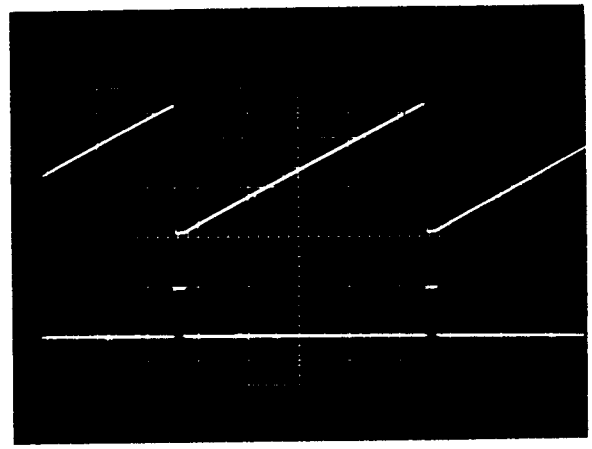


Figure 6.1. Constant Current Ramp Generator.

Upper trace — output (2V/cm)
Lower trace — input (5V/cm)
Horizontal scale — 200µS/cm



Waveforms

This method uses the high output impedance of transistor Tr2 to give a close approximation to constant current charging, the current being defined by R1, R2 and R3. Tr3 provides a low impedance output and component values for this stage must be chosen so that the base current of Tr3 is very much less than the charging current.

In the circuit of Figure 6.1, Tr3 runs at 2mA and requires a base current of 20µA maximum (10µA typical) and for non-linearity to be negligible the charging current should be about 1mA.

For a ramp of 1mS duration and 5V amplitude:

$$CV = IT \text{ therefore } C = \frac{IT}{V} = \frac{10^{-3} \times 10^{-3}}{5}$$

$$= 0{\cdot}2\mu F.$$

The waveforms obtained are shown in Figure 6.1.

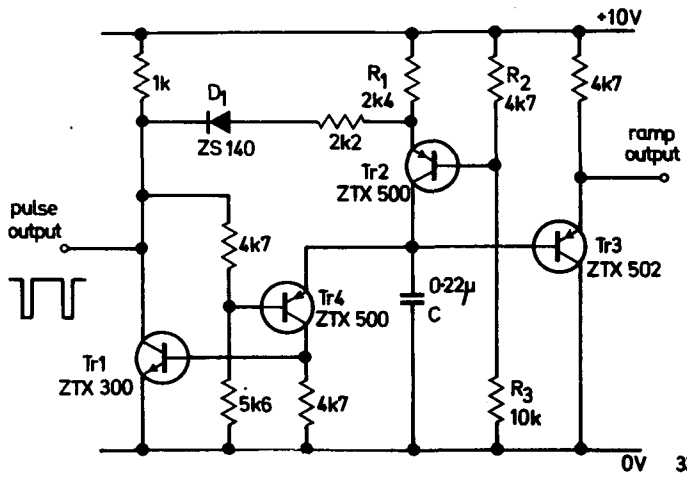


Figure 6.2

A self oscillating version of Figure 6.1.

A synchronising signal can be applied to the base of Tr4.

Figure 6.2 shows how the circuit can be modified so as to be self-oscillating. The output waveform obtained is virtually the same as for Figure 6.1. The timing capacitor charges until its voltage exceeds the base voltage of Tr4 by 0·7V. Tr4 then conducts and as Tr1 starts to conduct the base voltage of Tr4 falls, providing regenerative feedback. Tr1 and Tr4 saturate and rapidly discharge the capacitor to approximately 0·7V. Diode D1 cuts off the current source so that as soon as C has been discharged Tr1 and Tr4 turn off and the linear charge starts again. Ramp times down to 10μS can be obtained by choice of a suitable capacitor, and down to 1μS if Tr1 and Tr4 are replaced with ZTX310 and ZTX510 respectively.

Boostrap Ramp Generator

Waveform

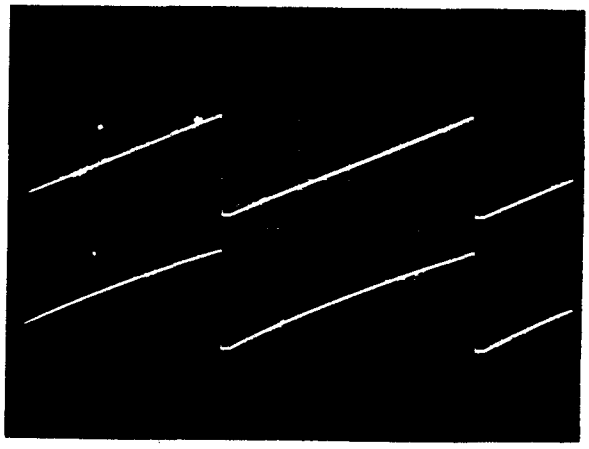
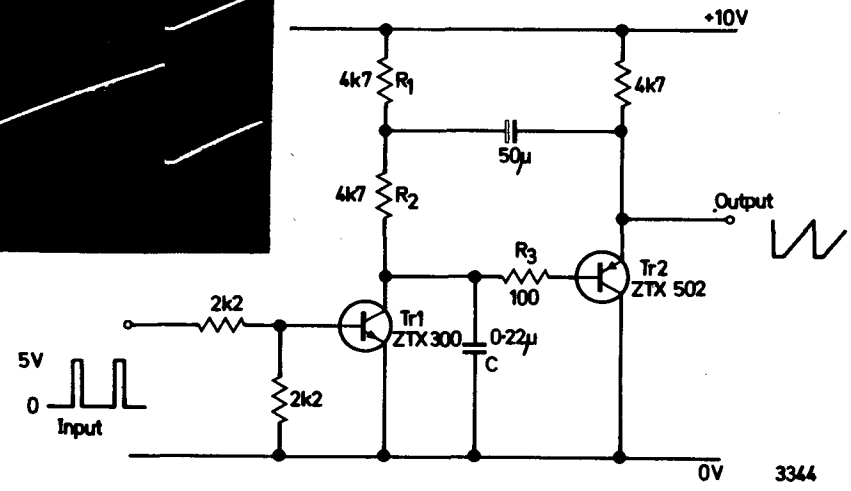


Figure 6.3



Upper trace —with boostrap capacitor (2V/cm)
Lower trace —without boostrap capacitor (2V/cm)
Horizontal scale —200 μS/cm

If the voltages at both ends of a resistor change by the same amount there will be no change in current. This is basically what the boostrap circuit does. Figure 6.3 shows a practical circuit and the output waveforms obtained, resistors R1 and R2 replacing the current generator of Figure 6.1 and providing a charging current of 1mA. R3 is a parasitic stopper.

Parabolic Correction

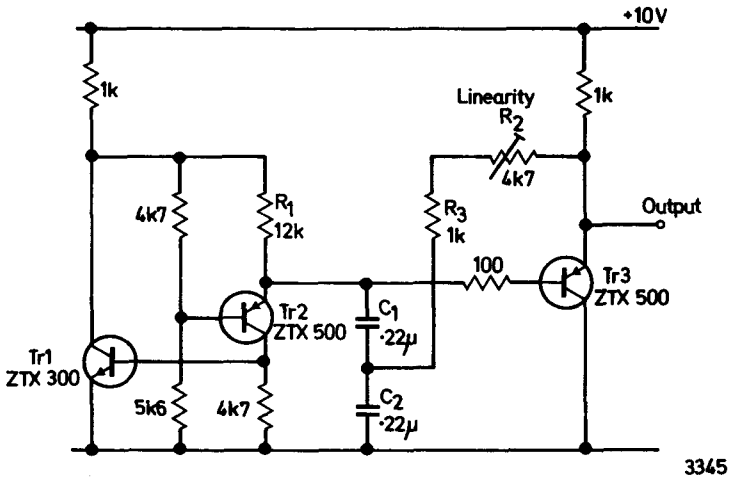


Figure 6.4

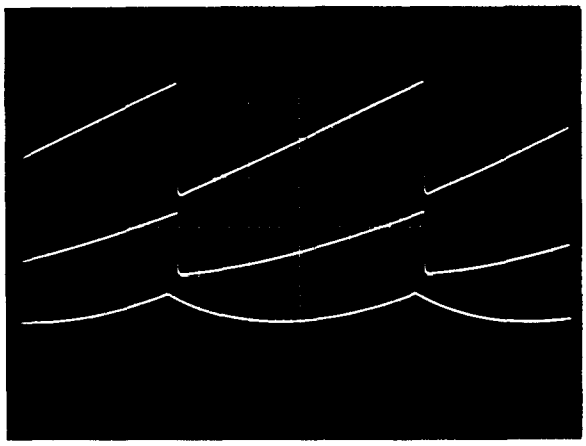
Ramp Generator with parabola correction.

Upper trace —output with R2 adjusted for best linearity (2V/cm).

Centre trace —waveform across C2 (2V/cm).

Lower trace —parabolic component of centre trace, obtained by cancelling sawtooth component (0·5V/cm).

Horizontal scale —200μS/cm.



Waveforms

If a sawtooth waveform is integrated with an R-C network a parabolic waveform is obtained. If the parabolic waveform is then added to an exponential ramp, in the correct proportions, the non-linearity of the ramp can be cancelled out.

Figure 6.4 shows a practical self-oscillating circuit employing this technique. R1 is the charging resistor and the timing capacitor is split into C1 and C2. C1 and C2 need not be equal, although this is often convenient. The output is fed back to C2 via R3 and the linearity control R2, and the integration is performed by the time constant of the components.

This type of circuit is particularly useful for field scan generation in television receivers since the facility of adjustable linearity allows non-linearity in the field output stage to be corrected.

Feedback Integrator

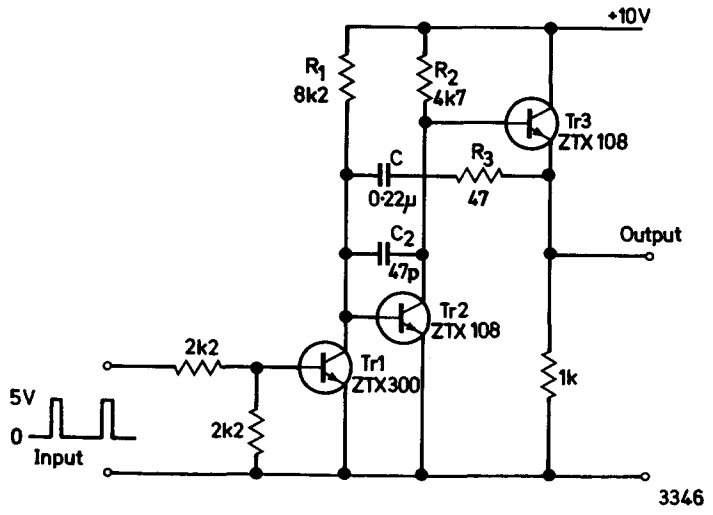
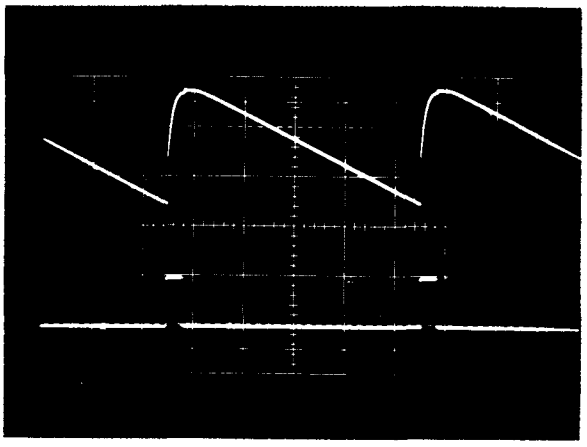


Figure 6.5

Ramp Generator using feedback integrator.

Upper trace —output (2V/cm).
Lower trace —input (5V/cm).
Horizontal scale —200μS/cm.



Waveforms

Assume that initially Tr1 is saturated and Tr2 is cut-off. When Tr1 turns off the current flowing in the charging resistor R1 flows into the base of Tr2 which starts to conduct. Its collector voltage and the emitter voltage of Tr3 fall, and a current flows through C to offset that provided by R1. Since the base voltage of Tr2 remains virtually constant the current in R1 remains constant and the capacitor discharges linearly until the re-set pulse arrives. Tr1 then saturates, Tr2 is cut off, and C recharges rapidly via Tr1, R3 and Tr3. R3 limits the recharging current to a safe value. For good linearity the base current required by Tr2 should be much less than the charging current. One disadvantage of the circuit shown is that there is a slight delay before the start of the ramp to the need to charge C through V_{be} before Tr2 starts to conduct. C2 is a parasitic stopper.

A Field Scan Generator for Vidicon Tubes

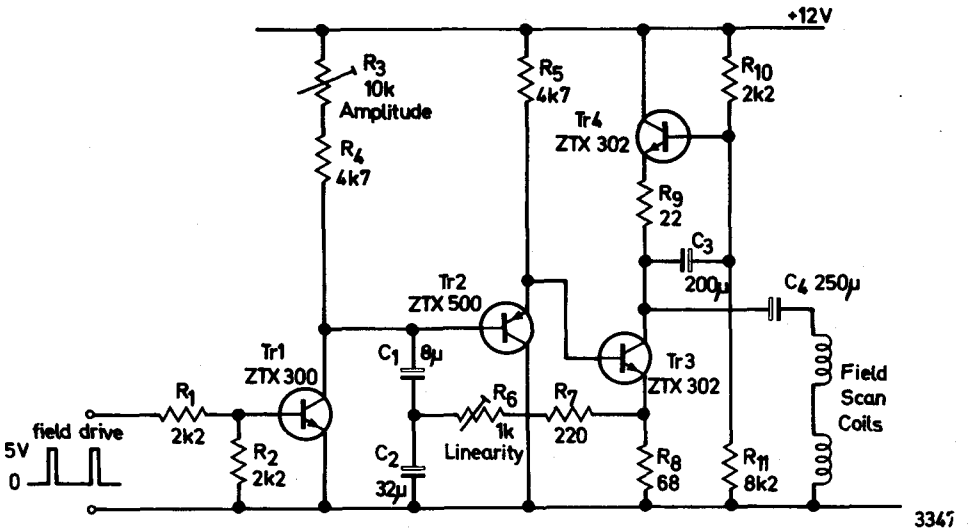
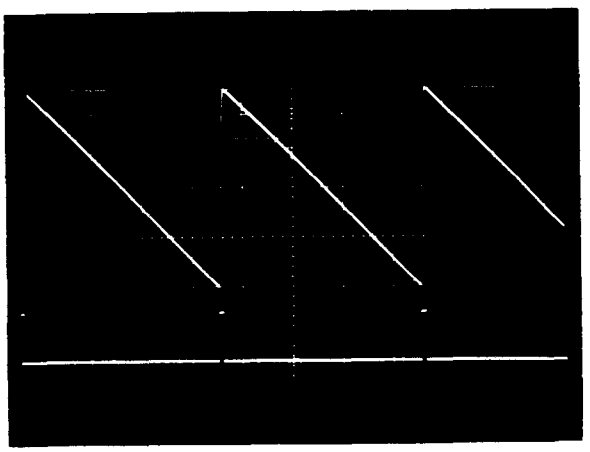


Figure 6.6



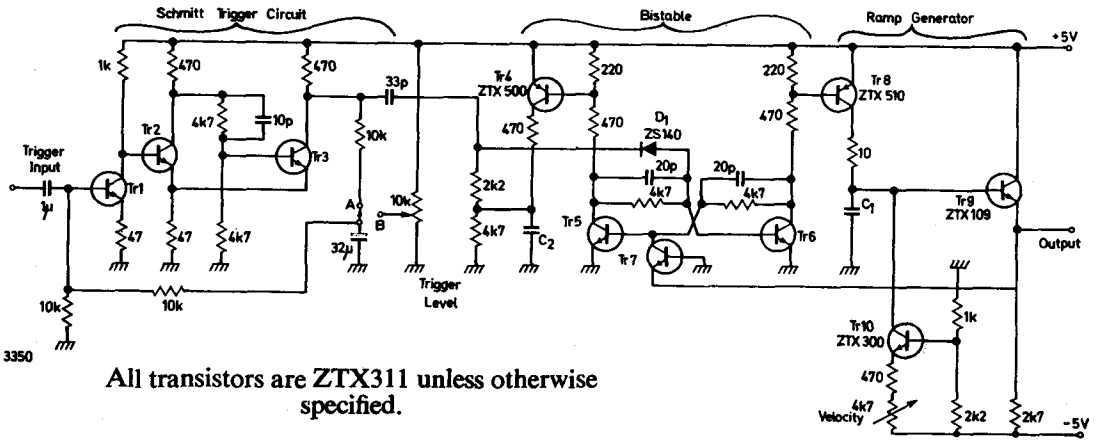
Upper trace —output current (10mA/cm).
Lower trace —field drive (5V/cm).
Horizontal scale —5mS/cm.

Waveforms

Field scan coils used with 1" vidicon tubes usually have a resistance of about 160Ω, inductance of 40mH, and require 30-40mA pk-pk scan current. A practical circuit is shown in Figure 6.6

The circuit requires an input pulse of 1mS period, +5V amplitude and 20mS repetition time. Tr1 discharges the timing capacitors C1 and C2, and R3 controls the charging current and hence the amplitude of the sawtooth generated. Emitter follower Tr2 increases the input impedance of Tr3 and also compensates for its V_{be}. The emitter current of Tr2 was chosen to be about four times the peak base current required by Tr3. Tr3 and Tr4 together form a high impedance output stage. The upper transistor Tr4 is an emitter follower for d.c. conditions and allows the bias voltage at the output to be defined by R10 and R11. Under a.c. conditions capacitor C3 effectively shorts the base to point "A" and the current flowing in Tr4 remains constant. Tr3 is a common emitter amplifier with a large amount of local negative feedback provided by R8. This gives Tr3 good linearity and a very high output impedance, and also provides a convenient source for the parabola correction. The value of R8 was chosen to give 40mA pk-pk scan current with about 3 volts pk-pk input. A higher value would give improved linearity but would reduce the available output swing (the scan coils require 6·5V pk-pk at 40mA) and a lower value would give more output but inferior linearity. When electrolytic capacitors are used for C1 and C2 the first part of the ramp may be non-linear so very low ramp amplitudes are undesirable.

A Wide Range Oscilloscope Timebase



All transistors are ZTX311 unless otherwise specified.

Figure 6.7

	Speed Range	C1	C2
1	1µS–10µS	1000pF	100pF
2	10µS–100µS	·01µF	1000pF
3	100µS–1mS	·1µF	·01µF
4	1mS–10mS	1·0µF	·1µF
5	10mS–100mS	10µF	1·0µF

Note. Values of C1 and C2 were chosen so that only one bank of capacitors is required, i.e. C1 on range 1 becomes C2 on range 2, etc.

The circuit shown in Figure 6.7 is intended for oscilloscope time bases and it will generate a linear ramp of 5V amplitude over a range of 100mS to 1µS. It will synchronize up to at least 30MHz with 20mV trigger input.

Transistors Tr1, Tr2 and Tr3 form a trigger amplifier and Schmitt trigger circuit. With S1 in position A (as shown) the bias for Tr1 is derived from the output of the Schmitt trigger circuit, and in the absence of an input signal, the circuit oscillates continuously at about 50Hz. This keeps the ramp generator running and provides a base-line on the oscilloscope screen, and also biases Tr1 for maximum sensitivity. With an input of more than 10mV r.m.s. (sinewave) the circuit triggers normally at signal frequency. In the "B" position a d.c. bias is applied to Tr1 for triggering from low frequency or non-periodic waveforms.

Tr5 and Tr6 form a bistable, and Tr8, Tr9 and Tr10 form a constant current type ramp generator. Assume that initially Tr6 is on, Tr7 is off and the re-set transistor Tr8 has fully recharged C1. The first trigger pulse from the Schmitt trigger circuit cuts off Tr6, the bistable changes state and Tr8 turns off allowing C1 to discharge linearly at a rate determined by VR2. At the same time Tr4 turns on and reverse biases the trigger diode so that no further trigger pulses can reach Tr6. When the emitter voltage of Tr9 falls to –0·7V Tr7 starts to conduct and turns off Tr5. The bistable then re-sets to its original state and C1 rapidly recharges through Tr8. Meanwhile Tr4 has turned off and the voltage across C2 decays until it is low enough for trigger pulses to reach Tr6. The cycle then repeats.

Staircase Generators

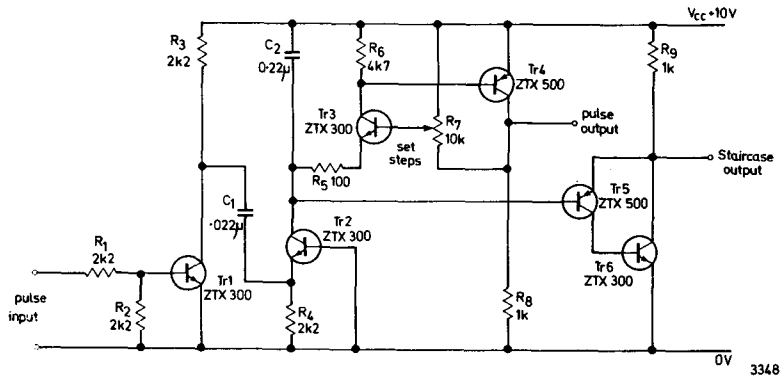


Figure 6.8

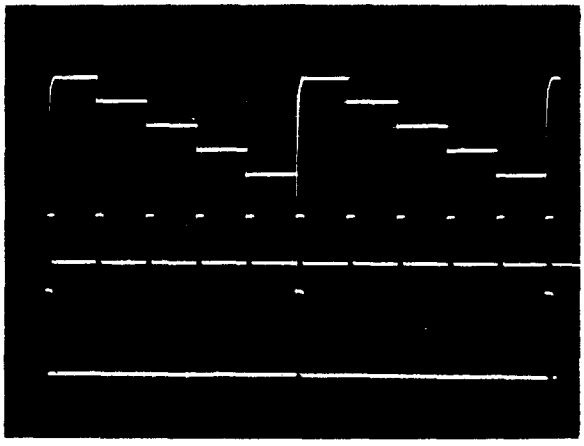
Input frequency range—50Hz-2kHz.

Top trace—output waveform with 4 steps (2V/cm).

Centre trace—input waveform (5V/cm).

Bottom trace—output pulse from Tr4 (5V/cm).

Horizontal scale—1mS/cm.



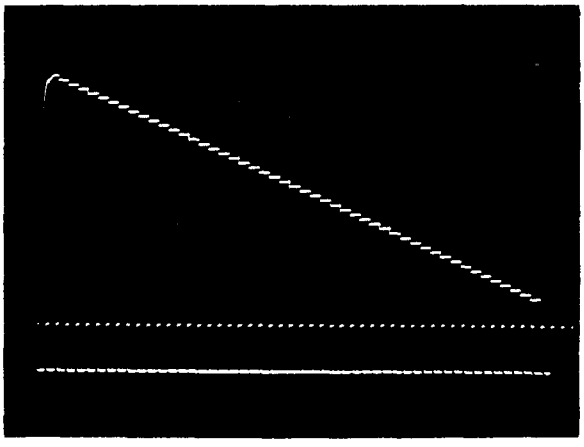


Figure 6.9

Output waveform with 50 steps, obtained by reducing C1 to 2200pF.

Input frequency —10kHz
Upper trace —Output 1V/cm
Lower trace —Input 5V/cm
Horizontal scale —500μS/cm

A staircase waveform can be obtained by charging a capacitor with current pulses. Figure 6.8 shows an example. When Tr1 turns off, C1 charges up to V_{cc} via R3 and R4 and stores charge $Q1 = C1\ V_{cc}$. When Tr1 turns on the emitter of Tr2 is forward biased and the charge stored on C1 is transferred to C2. At each pulse the voltage across C2 increases by approximately $\frac{Q1}{C2} = \frac{C1\ .\ V_{cc}}{C2}$. Transistors Tr3 and Tr4 discharge C2 every time the collector voltage of Tr2 falls below the pre-set level on the base of Tr3. Tr5 and Tr6 form a high gain compound emitter follower which isolates the output from C2.

With the component values shown, the circuit will generate a staircase of 2-10 steps with an input pulse rate of 50Hz-2kHz. Figure 6.9 shows a 50-step staircase generated by replacing C1 with a 2200pF capacitor. The input pulse rate in this case was 10kHz.

The staircase generator can be used as a simple frequency divider if Tr5 and Tr6 are omitted and the output is taken from the collector of Tr4. Division ratios of more than about five are not recommended, in the interests of stability.

Pulse Counters

A pulse counter gives an output voltage, or current, proportional to the input frequency. Figure 6.10 shows an example, and the similarity between this and the staircase generator will be evident. When Tr1 turns on, C1 charges via Tr1 and D1, and stores charge Q = C1 . V_{cc} (approximately). When Tr1 turns off, C1 discharges through R3 and the emitter of Tr2 and the charge of C1 is transferred to the collector circuit of Tr4, giving a mean current of $i = \frac{Q}{t} = Q \cdot f$, where f is the input frequency.

i.e. for f.s.d. of a 1mA meter at 100kHz with V_{cc} = 10V.

$$i = Q \cdot f, \text{ therefore } Q = \frac{i}{f} = \frac{10^{-3}}{10^{5}} = 10^{-8} \text{ coulombs.}$$

$$C1 = \frac{Q}{V_{cc}} = \frac{10^{-8}}{10} = 10^{-9} \text{ farads i.e. 1000pF.}$$

In practice a slightly higher value of C1 or V_{cc} is required due to the voltage drop across D1. Care must be taken that C1 can discharge completely in the time for which Tr1 is turned off, i.e. at 100kHz Tr1 will be turned off for 5μS (square wave) therefore C1 . R3 $\leqslant$ 5μS for C1 to discharge to 1% of V_{cc}, i.e. R3 $\leqslant$ 1kΩ.

The circuit shown in Figure 6.10 will operate over the range of 10Hz-1MHz by choice of C1 with a linearity of 2% of full scale on the lower ranges and 5% of full scale on the 100kHz-1MHz range. It can be calibrated either by adjustment of the supply voltage or by an adjustable meter shunt.

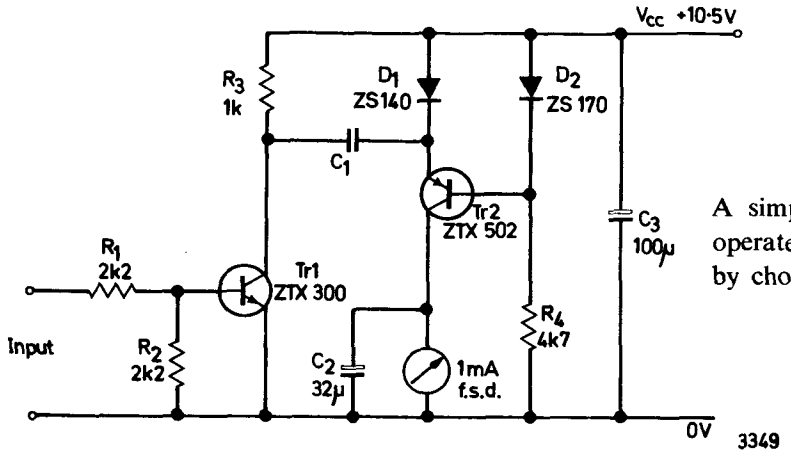


Figure 6.10

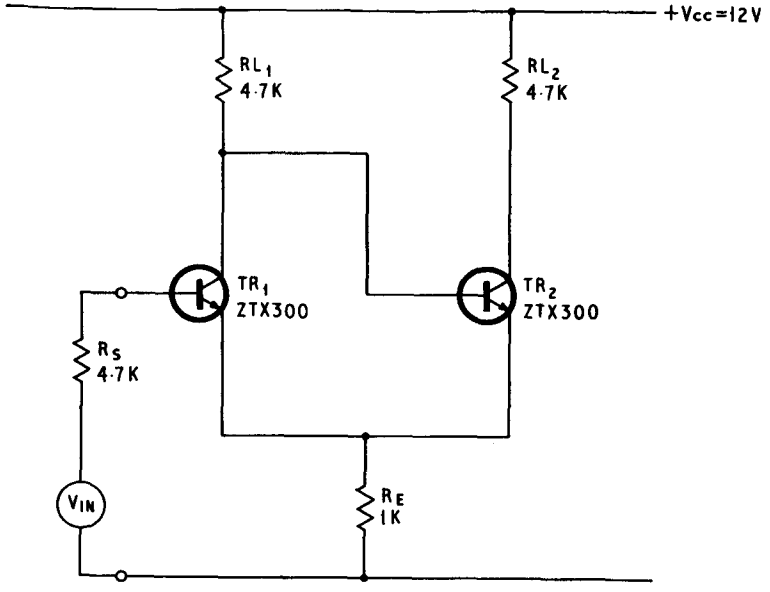
A simple pulse counter which will operate over the range 10Hz-1MHz by choice of a suitable value of C1.

Frequency range	C1
10Hz–100Hz	1·0μF
100Hz–1kHz	0·1μF
1kHz–10kHz	0·01μF
10kHz–100kHz	1000pF
100kHz–1MHz	100pF

SECTION 7
SCHMITT TRIGGER CIRCUITS

The Schmitt Trigger Circuit is a useful level operated switch. Feedback via the common emitter resistor causes the circuit to switch rapidly from on to off and vice versa.

The circuit of Figure 7.1 has two states. One state is with Tr1 on and Tr2 off, and the other with Tr1 off and Tr2 on. If V_{in} is increased from zero, when the transition voltage VT_1 is reached, Tr1, which was non-conducting, now starts conducting, cutting off Tr2, and the circuit rapidly changes state if the loop gain is greater than unity. If the loop gain is less than unity the circuit will slowly change states and can be stopped with both transistors conducting. If V_{in} is now reduced, when the second transition voltage VT_2 is reached, the current through Tr1 begins to reduce and regenerative action causes Tr2 to come on, turning off Tr1.



Tr1, Tr2 ZTX300 (BCW10).

Figure 7.1

It will be noted that V_{in} must be reduced to a value less than VT_1 for the circuit to revert to its former state. The difference between VT_1 and VT_2 is referred to as the hysteresis or backlash of the circuit.

Figure 7.2 shows the relationship between the collector current of Tr2 and V_{in}.

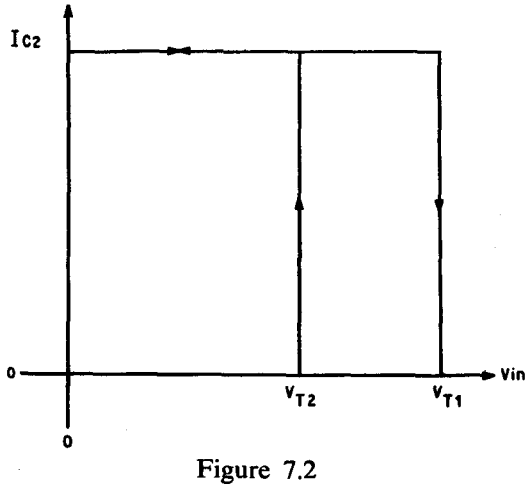


Figure 7.2

It is difficult to predict accurately the values of VT_1 and VT_2, but the approximate formulæ for VT_1 and VT_2 below may be of assistance to the circuit designer.

$$\text{The upper threshold } VT_1 \approx V_{BE1} + \left\{ \frac{V_{cc}(R_E R_{L2} + R_E R_{L1}) - V_{BE(sat)}(R_E R_{L2})}{R_{L1}R_E + R_E R_{L2} + R_{L2}R_{L1}} \right.$$

$$\text{The lower threshold } VT_2 \approx V_{BE1} + \frac{(V_{cc} - V_{BE2})\,R_E}{R_{L1} + R_E}$$

Assuming $V_{BE(sat)} = 0{\cdot}75V$ and $V_{BE1} = V_{BE2} = 0{\cdot}65V$ and that $R_s \ll R_{in}$

$VT_1 = 4{\cdot}12V$

$VT_2 = 2{\cdot}63V$

(V_{BE1} and V_{BE2} are the forward base-emitter voltage drops of Tr1 and Tr2 respectively when their collector currents are equal).

Measured values of VT_1 and VT_2 are 4·15V and 2·6V respectively.

High Speed Schmitt Trigger

The circuit of Figure 7.3 is a high speed Schmitt Trigger which operates from d.c. – 50 MHz. Storage delay times are eliminated by keeping the transistors out of saturation by operating in the current mode. Rise and fall times are < 6nS.

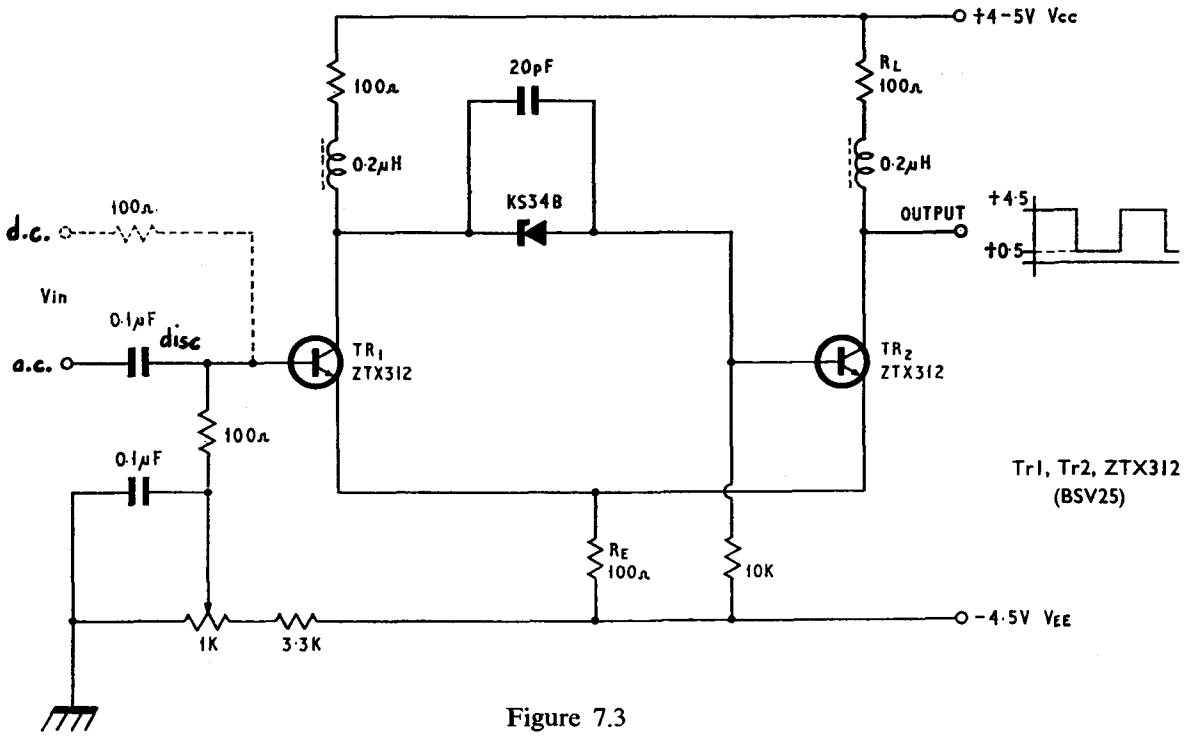


Figure 7.3

Upper trace—output waveform at 50MHz (2V/cm).

Lower trace—Output waveform at 10MHz (2V/cm).

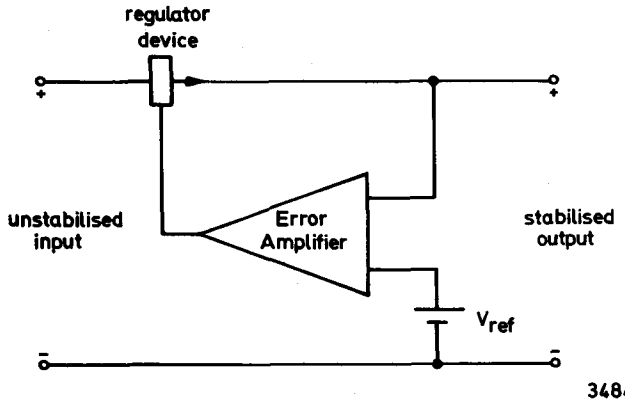
The zener diode keeps the base of Tr2 at about zero volts when Tr1 is "on", the emitter current being given by $\frac{V_{EE} - V_{BE}}{R_E}$. The values of V_{cc} and R_L are selected so that $\frac{V_{cc}}{R_L} > \frac{V_{EE} - V_{BE}}{R_E}$ and the transistor stays out of saturation.

The h.f. chokes are included to compensate for capacitive loading of the Schmitt and may be omitted if the loading is light. Sensitivity is 1·5V at 50 MHz.

SECTION 8

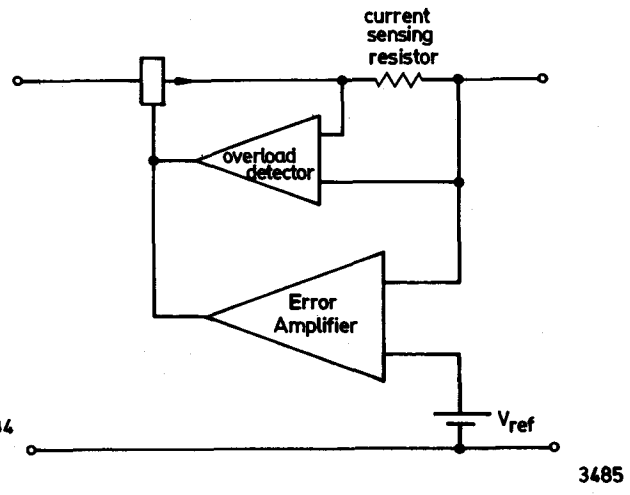
STABILISED POWER SUPPLIES

Most electronic circuits require power supplies, and it is usually desirable for the power to be obtained from the a.c. mains. To minimize ripple and to provide a stable supply voltage regardless of mains and load variations, a stabilised power supply is required. There are basically two types—series stabilizers and shunt stabilizers.



Basic series stabiliser.

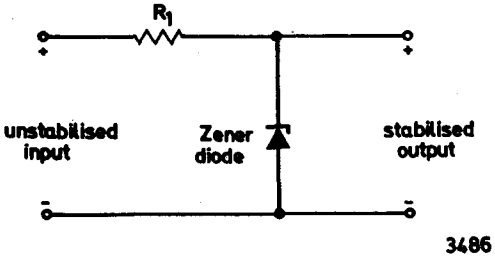
Figure 8.1



Series stabiliser with current limit.

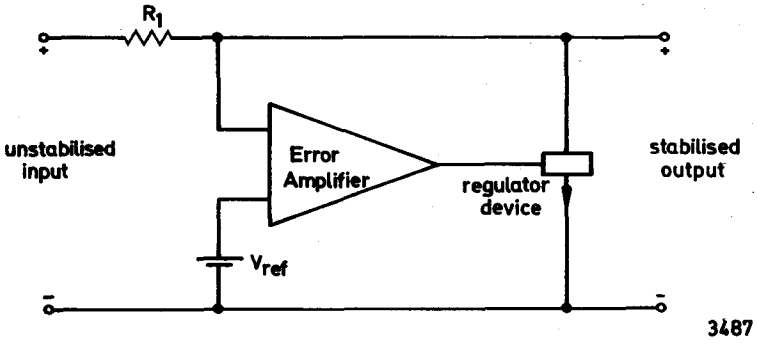
Figure 8.2

In the series stabilizer, shown in Figure 8.1, the regulator device is put in series with the load. An error amplifier compares the output voltage with a reference source—usually a zener diode—and controls the current flowing in the regulator device so as to minimize the error. The power dissipated in the regulator is very low with no load and rises to a maximum between half and full load. There is no inherent short circuit protection but this can be provided by additional circuitry as shown in Figure 8.2.



Simplest form of shunt stabiliser.

Figure 8.3



Shunt stabiliser with error amplifier.

Figure 8.4

In the shunt stabilizer, the simplest form of which is a single zener diode, Figure 8.3, the regulator element is placed in parallel with the load and is current fed by a series resistor. The error amplifier controls the current flowing through the regulator device to compensate for variations of supply of load current and maintain constant output voltage. The shunt stabilizer has inherent short circuit protection but its efficiency is low due to the power dissipated in the series resistor. For this reason it is normally only used in low current applications.

Figure 8.5 shows an extremely useful series stabilizer circuit which can be adapted to a wide range of output voltages and currents by choice of suitable components. The output voltage is fixed at 0·7V above the zener voltage of D1. In most cases it will be necessary for Tr2 to be a Darlington pair of a low power transistor and a high power type due to the power dissipation. The approximate design procedure is as follows assuming ±10% mains variation.

A 12V 1A Power Supply

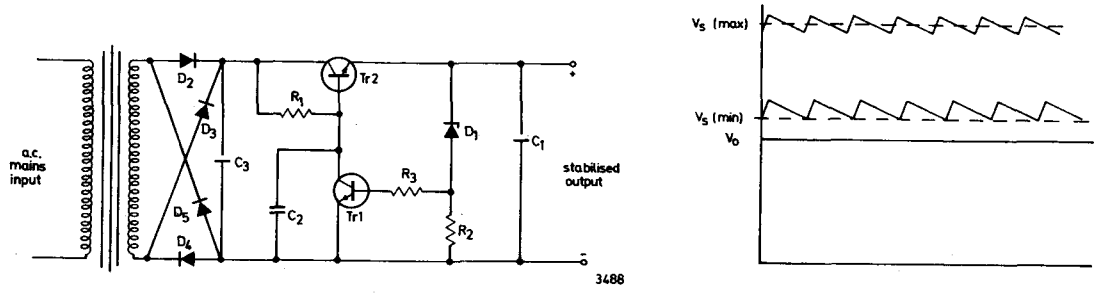


Figure 8.5. A practical series stabiliser circuit, with unstabilised input conditions for high and low mains voltage.

(1) Choose zener diode to give output voltage as near as possible to that required; i.e. for 12V nominal output an 11V zener (KS110A) would give 11·7V.

(2) Estimate the minimum input voltage as 10% or 2V higher (whichever is the greater) than the required output. This must be measured to the bottom of the ripple waveform as shown in Figure 8.5. For 12V output the minimum input voltage would be 14V.

(3) Choose a suitable value of smoothing capacitor, so that the ripple voltage is not more than about 10% of the output voltage; i.e. for a 1A output at 12V the minimum ripple would be about 1·2V pk-pk. For a full wave rectifier $CV = IT$, therefore $C = \frac{I.T}{V} = \frac{1 . 10^2}{1 . 2} = 8000\mu F$.

In practice the finite winding resistance of the mains transformer tends to reduce the ripple and a smaller value can be used. A 5000-6000μF capacitor would be suitable for this case.

(4) It is rather difficult to calculate the output voltage required from the mains transformer secondary because the regulation of the transformer varies considerably according to manufacturer, core material and size.

As a rough guide the worst case output voltage can be taken as:

$V_{s(min)} = (V \text{ r.m.s.} \times \sqrt{2} \times 0{\cdot}8) - V_r - V_d$

where V_s = unstabilised supply voltage (14V min. in above case)

V r.m.s. = Nominal secondary voltage.

V_r = ripple voltage (1·2V in above case)

V_d = voltage drop in rectifiers. (1V for two phase full wave)
(2V for bridge full wave)

the 0·8 factor allows for 10% mains reduction and 10% transformer regulation.

If we assume a bridge rectifier.

$$V \text{ r.m.s.} = \frac{V_{s(min)} + V_r + V_d}{\sqrt{2} \times 0{\cdot}8} = \frac{14 + 1{\cdot}2 + 2{\cdot}0}{\sqrt{2} \times 0{\cdot}8} = 15{\cdot}2V \text{ r.m.s.}$$

In many cases it will be necessary to use a "stock" transformer and the voltage chosen should then be the nearest available on the high side of the calculated value.

(continued overleaf)

(5) In order to calculate the power dissipation in the transistors used, the maximum supply voltage must be known. This can be estimated from:

$$V_{s(max)} = (V \text{ r.m.s.} \times \sqrt{2}) - \frac{V_r}{2} - V_d.$$

This allows for 10% rise due to mains variation and a 10% fall due to load regulation, the two factors cancelling out. If we use a "stock" transformer with a 17V r.m.s. secondary

$V_{s(max)} = (17 \times \sqrt{2}) - 0{\cdot}6 - 2{\cdot}0 = 21{\cdot}4$ volts (average).

The supply voltage with no load will be approximately 10% higher than this; i.e. 24 volts, and the voltage rating of the reservoir capacitor C1 should exceed this by at least 20%.

(6) The minimum supply voltage with a 17V transformer will be:

$$V_{s(min)} = (17 \times \sqrt{2} \times 0{\cdot}8) - 1{\cdot}2 - 2{\cdot}0 = 16 \text{ volts.}$$

(7) The power dissipation in the regulator device Tr2 will be $I_L \,.\, (V_{s(max)} - V_o)$ where I_L = the maximum load current, V_o = output voltage.

$$= 1 \,.\, (21{\cdot}4 - 11{\cdot}7) = 9{\cdot}7 \text{ watts.}$$

The current and power required necessitate a Darlington pair. The power transistor can be a 2N3055 which can easily handle the required current, voltage and power. To maintain a safe junction temperature at ambient temperatures up to 50°C, the thermal resistance of the heat-sink should not exceed 10°C/watt.

(8) If we assume a minimum current gain of 30 at 1A, the base current of the power transistor will be 33mA and the maximum power dissipation in the driver transistor (Tr3 in Figure 8.6) will be $\frac{9{\cdot}7}{30} = 323\text{mW}$. This is within the capabilities of a BFS59 for ambient temperatures up to 75°C.

(9) The maximum base current required by the BFS59 will be $\frac{33\text{mA}}{h_{FE(min)}}$; i.e. $0{\cdot}83\text{mA} = I_b$.

(10) The resistor R1 must be able to supply this current at the minimum supply voltage, $V_{s(min)}$, of 16 V.

$$R1_{(max)} = \frac{V_{s(min)} - V_o - V_{be2} - V_{be3}}{I_b}$$

Assuming $V_{be2} = 1{\cdot}0\text{V}$ and $V_{be3} = 0{\cdot}7\text{V}$

$$R1_{(max)} = \frac{16 - 11{\cdot}7 - 1{\cdot}0 - 0{\cdot}7}{0{\cdot}83 \times 10^{3}}$$

$$= 3{\cdot}13\text{k}\Omega$$

If we allow for a 20% end of life tolerance on R1 its nominal value will be 2·6kΩ. The nearest preferred value is 2·4kΩ.

(11) With R1 at the low end of its tolerance its value will be 1·92kΩ, and with the maximum (off load) supply voltage of 24 volts the current will be 5·5mA. The power dissipation in Tr1 will hence be $5{\cdot}5 \times 13{\cdot}4 = 74\text{mW}$. This is well within the ratings of a ZTX108. If the current in R1 was found to be excessive with maximum supply voltage it would be necessary to re-design for a higher transformer output or to use higher gain transistors.

(12) R2 is chosen to give a zener current of 5mA, this being the current at which the zener voltage is specified. For $V_{be1} = 0{\cdot}7\text{V}$, R2 = 140Ω nominal (150Ω preferred).

(13) R3 is chosen to limit the base current to Tr1 to a safe value under fault conditions. It should be as small as possible and a suitable value is 47Ω. R4 is chosen to shunt away the collector base leakage current of the 2N3055. A value of 470Ω is suitable and the extra current required from Tr3 is negligible (2mA).

(14) C1 reduces the output impedance of the power supply at high frequencies (above 10kHz), 250μF is a suitable value. C2 is chosen to suppress h.f. oscillation. Its minimum value should be determined on test, 0·01μF will usually be sufficient.

(continued)

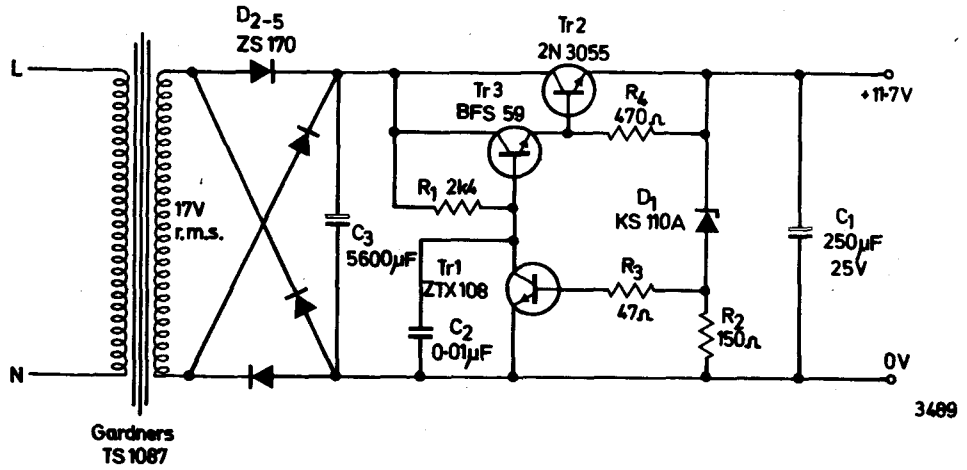


Figure 8.6. A 12V, 1A power supply circuit.

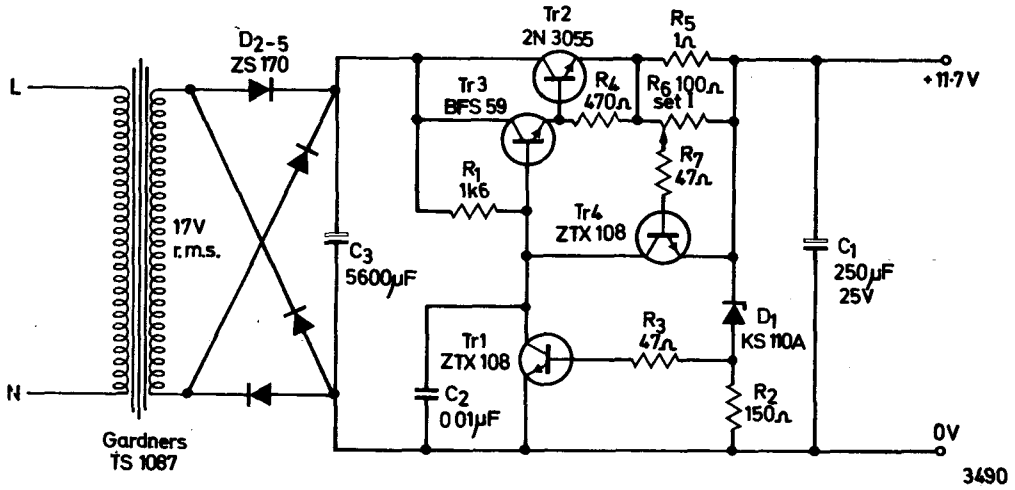
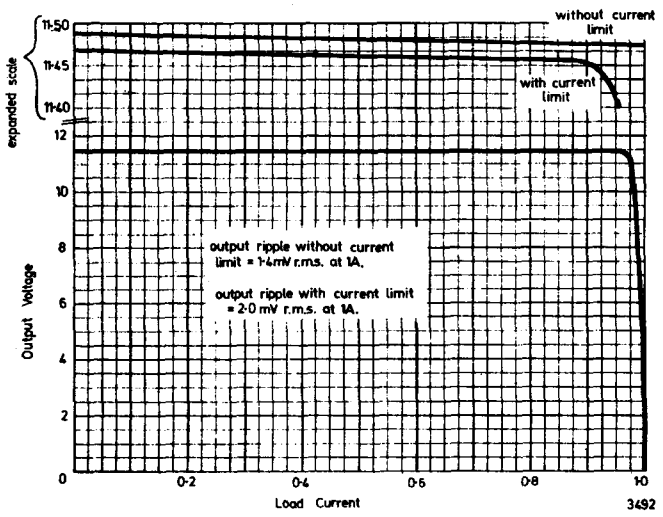


Figure 8.7. A 12V, 1A power supply circuit with current limit.



Output voltage/load current graph for the 12V, 1A power supply.

When a current limit is required this can be provided as shown in Figure 8.7. When the V_{be} of Tr4 exceeds 0·7V, Tr4 starts to conduct and diverts base current from Tr3, hence limiting the output current to a pre-set value. The component values required can be calculated as follows:

(15) Choose R5 to drop about 1 volt at maximum output current. For 1A output, R5 = 1Ω.

(16) Recalculate R1 allowing for the additional 1V drop across R5. This will also increase the minimum supply voltage $V_{s(min)}$ by 1V. Using a 17V r.m.s. transformer as before,

$$V_{s(min)} = 16V$$

$$R1_{(max)} = \frac{16 - V_o - V_{be2} - V_{be3} - I}{I_b}$$

$$= 1{\cdot}93k\Omega.$$

Hence the maximum nominal value of R1, assuming 20% ultimate tolerance, is 1·6kΩ.

(17) R7 is chosen to limit the base current of Tr4 to a safe value under fault conditions. 47Ω is suitable.

(18) The transistor operates under low voltage, low current conditions, type ZTX108 is suitable.

A 0-30 Volt Variable Power Supply

This circuit will give an output voltage which can be adjusted between 0 and 30 volts, at up to 1 amp. It has current limiting overload protection.

Tr5 and Tr6 form the error amplifier. The voltage on Tr6 base is compared with that on Tr5 (zero) and the difference is further amplified by Tr3 which controls the regulator device Tr1-2. As the voltage at point A must always remain close to earth, the current flowing through R2 and R3 must remain constant. If the base current of Tr6 is neglected this same current flows through R1 so that the output voltage $V_o = V_r \times \frac{R1}{R2 + R3}$ i.e. the output voltage is directly proportional to R1, which can be a wirewound potentiometer or a bank of fixed resistors selected by switches.

The reference voltage is provided by D10. The KS051A being chosen for its low temperature coefficient. Tr4 provides overload protection in the same way as previously.

D.C. output resistance is approximately 10mΩ and there is 0·1% change in output voltage for a ±10% change in mains voltage. Ripple at 10V output and 1A load is 1·5mV r.m.s.

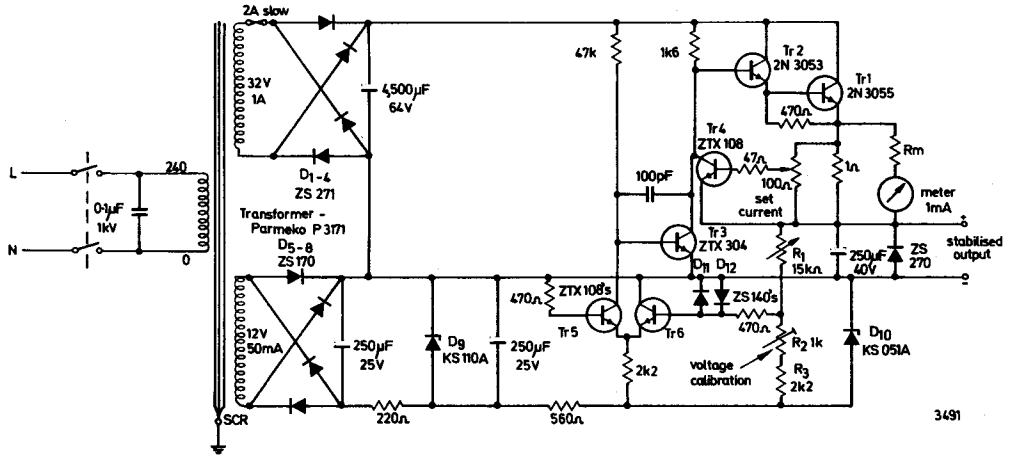


Figure 8.8. A 0-30V, 1A variable power supply.

Note: Transistor Tr1 should be mounted on a heatsink of not more than 2°C/watt thermal resistance. Transistor Tr2 should be fitted with a heat dissipating clip, e.g. Redpoint 5F.

R_m is chosen to give a full-scale deflection of 1 volt on the output current meter, i.e. R_m = 900Ω if the meter resistance = 100Ω.

Operational Amplifier Power Supply

Figure 8.9 shows a simple ±15 volt power supply which will give up to 30mA output, for up to six ZLD709 operational amplifiers. It uses basically the same circuit as the 12V power supply described earlier.

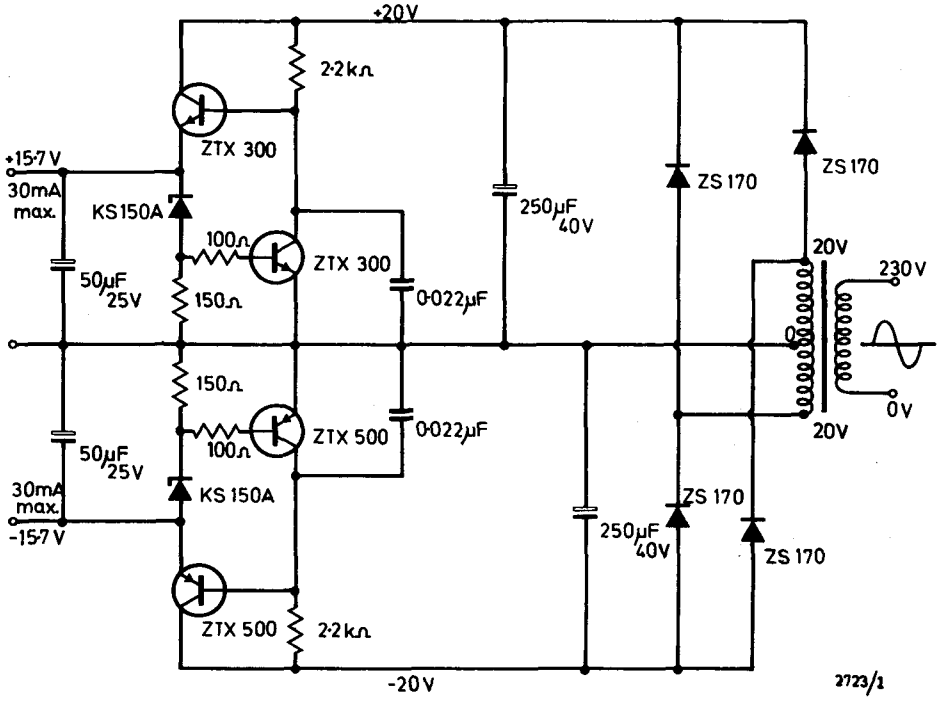
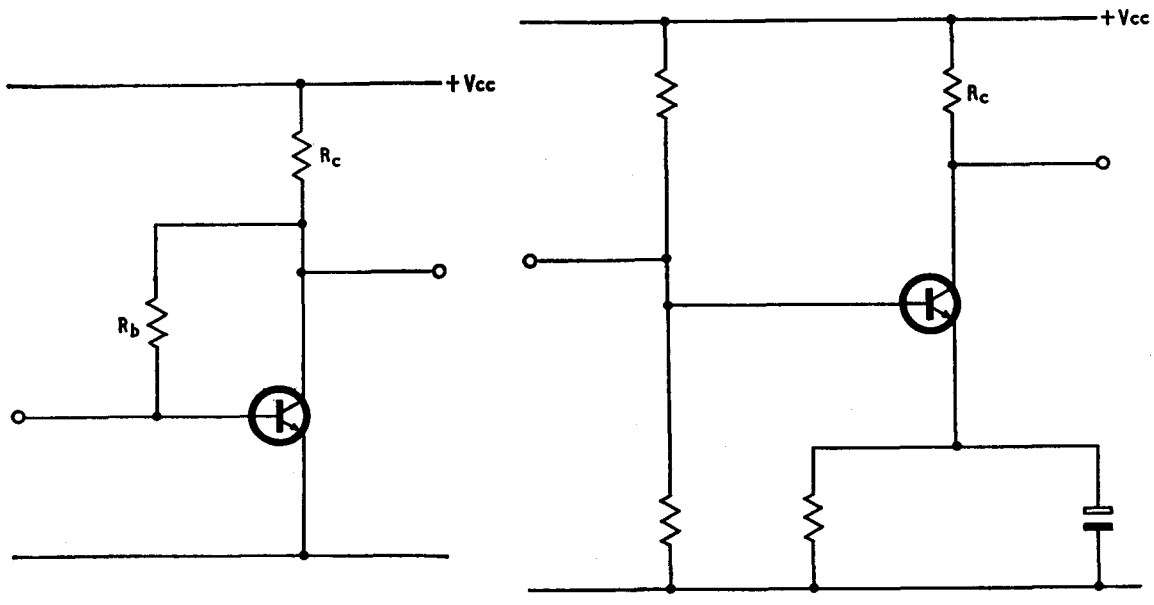


Figure 8.9

SECTION 9

AMPLIFIER CIRCUITS



Figures 9.1a, 9.1b

Figures 9.1a and 9.1b show two methods of biasing a simple transistor amplifier stage. Method (b) is widely used with germanium devices, and is necessary because of their significant collector-base leakage current. In silicon transistors I_{cbo} is usually negligible and the performance of Figure 9.1a is adequate for most applications, with a saving of two resistors and one electrolytic capacitor.

Usually the circuit is designed so that the collector voltage V_{ce} is approximately half of the supply voltage V_{cc}. This is achieved when:

$$R_b = h_{FE} R_c$$

where h_{FE} is the d.c. current gain of the transistor. In practice a wide range of current gains is encountered (e.g. ZTX300 h_{FE} =50-300 at 10mA collector current) so a value of h_{FE} given by:

$$h_{FE} = \sqrt{h_{FE(max)} \times h_{FE(min)}}$$

is used.

e.g. for a ZTX300 (BCW10)

$$\left.\begin{array}{l} h_{FE(max)} = 300 \\ h_{FE(min)} = 50 \end{array}\right\} \quad \therefore h_{FE} = \sqrt{50 \times 300}$$

$$h_{FE} = 122{\cdot}5$$

The choice of R_c depends upon the supply voltage and the amplification of the stage. For low level amplification a low value of collector current (50-300μA) is necessary to minimise noise and R_c will have a high value, of the order of 47kΩ. For wide-band amplification a low value of R_c is necessary to minimise the effect of stray capacitance, and a correspondingly high collector current (e.g. 10mA) is used to maximise f_T.

Example of D.C. Design for a Single Stage Amplifier

$I_c = h_{FE} I_b$

I_e (= current in R_c) $= I_c + I_b = I_b . (h_{FE} + 1) \approx h_{FE} I_b$ since $h_{FE} \gg 1$

$\therefore I_e \approx I_c = h_{FE} I_b$

$$I_b = \frac{V_{ce} - V_{be}}{R_b} \approx \frac{(V_{cc} - h_{FE} I_b R_e) - V_{be}}{R_b}$$

$$= \frac{V_{cc}}{R_b} - \frac{h_{FE} I_b R_e}{R_b} - \frac{V_{be}}{R_b}$$

$$\therefore I_b \left(1 + \frac{h_{FE} R_c}{R_b}\right) = \frac{V_{cc} - V_{be}}{R_b}$$

$$I_b = \frac{V_{cc} - V_{be}}{R_b \left(1 + \frac{h_{FE} R_c}{R_b}\right)} = \frac{V_{cc} - V_{be}}{R_b + h_{FE} R_c}$$

$$\therefore I_c = h_{FE} I_b = \frac{h_{FE} (V_{cc} - V_{be})}{R_b + h_{FE} R_c}$$

and $V_{ce} = V_{cc} - I_c R_c$

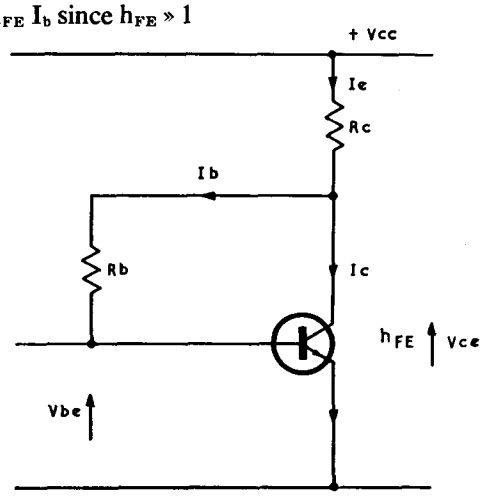


Figure 9.2

Let $V_{cc} = 10V$ and $R_c = 1k\Omega$

Transistor is a ZTX300 (BCW10)

$\therefore h_{FE} = \sqrt{h_{FE(max)} . h_{FE(min)}} = \sqrt{50 \times 300} = 122{\cdot}5$

$\therefore R_b = 122{\cdot}5k = 120k\Omega$ preferred ($h_{FE} \times R_c$)

$$\therefore I_e = \frac{h_{FE} (V_{cc} - V_{be})}{R_b + h_{FE} R_c}$$

$$= \frac{122{\cdot}5 \ (10 - 0{\cdot}7)}{120 + (122{\cdot}5 \times 1)} \text{ mA}$$

$$= \frac{122{\cdot}5 \times 9{\cdot}3}{242{\cdot}5} = 4{\cdot}7\text{mA}$$

$\therefore$ collector voltage $= 10 - (4{\cdot}7 \times 1) = 5{\cdot}3$V nominal.

In practice the current gain of the transistor may lie between 50 and 300 and the resistor values may be (say) 20% higher or lower than their nominal values.

There are two worst case conditions (assuming constant supply voltage).

(1) h_{FE} is a minimum (50), R_c is a minimum (800Ω)
R_b is a maximum (144kΩ).

$$I_c = \frac{50 \ (10 - 0{\cdot}7)}{144 + (50 \times 0{\cdot}8)} \text{ mA}$$

$$= \frac{50 \times 9{\cdot}3}{188} = 2{\cdot}47\text{mA}$$

$V_{ce} = 10 - (2{\cdot}47 \times 0{\cdot}8) = 8{\cdot}0$ volts.

(2) h_{FE} is a maximum (300), R_c is a maximum (1·2k)
R_b is a minimum (96k)

$$I_c = \frac{300 \times 9{\cdot}3}{96 + (300 \times 1{\cdot}2)}$$

$$= \frac{300 \times 9{\cdot}3}{456} = 6{\cdot}14\text{mA}$$

$V_{ce} = 10 - (6{\cdot}14 \times 1{\cdot}2) = 2{\cdot}64$ volts.

In case (1) only two volts is dropped across the load resistance giving a maximum output of 4 volts peak to peak.

In case (2) the collector voltage can only fall by two volts before the transistor saturates, so the maximum output swing is again only 4 volts peak to peak.

For comparison, an output of nearly 9 volts peak to peak could be obtained with all values at the design centres. The possible variation in collector voltage could be minimised by using close-tolerance resistors and a narrow gain-spread transistor such as ZTX302 (BCW14).

Input Impedance

The input impedance of a transistor connected in the common emitter configuration is given approximately by $h_{fe} \times r_e$ where r_e is the intrinsic emitter resistance given by $r_e \approx \frac{25}{I_e}$ (Figure 9.3a)

I_e is the emitter current in mA

r_e is the emitter resistance in Ω

when an external emitter resistor is added the input impedance becomes $h_{fe}(r_e + R_e)$. (Figure 9.3b)

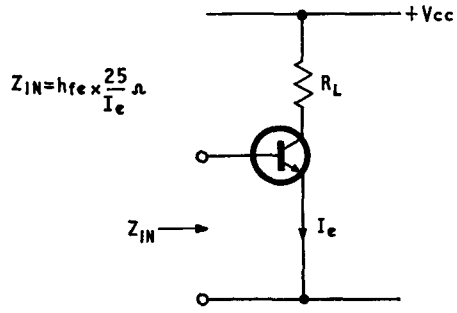


Figure 9.3a

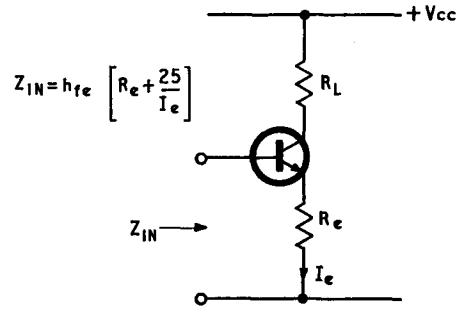


Figure 9.3b

Voltage Gain

Voltage gain = current gain × impedance gain

$$\approx \frac{h_{fe} \times R_L}{h_{fe}\, r_e} \approx \frac{R_L}{r_e} \left(\text{or } \frac{R_L}{r_e + R_e} \right)$$

i.e. voltage gain is independent of h_{fe}.

Feedback

In the simple bias circuit discussed earlier there is a small amount of voltage derived feedback, (i.e. a feedback *current* is produced proportional to the output *voltage*), due to the bias resistor between base and collector. This feedback reduces both the input impedance and the overall current gain in the same ratio. The factor by which they are reduced is given by:

$$\frac{1}{1 + \frac{h_{fe}\, R_L'}{R_b}}$$

h_{fe} = transistor a.c. current gain

R_b = bias resistor

R_L' = effective a.c. load resistance i.e. collector resistor R_c in parallel with the input impedance of the next stage.

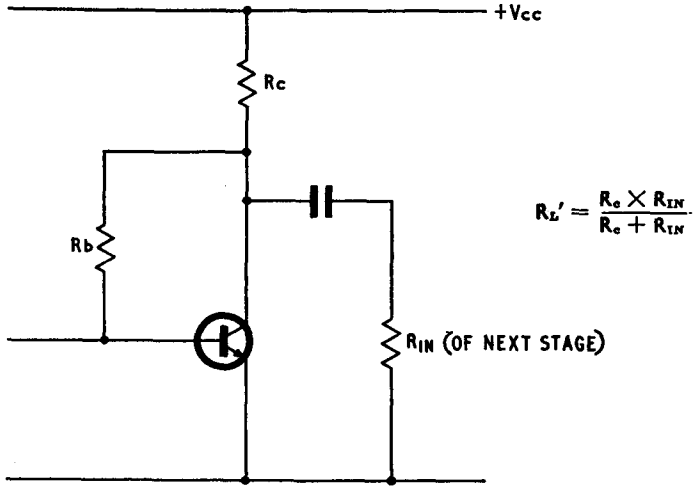


Figure 9.4

Current Feedback

When a resistance R_e is put in series with the emitter, a voltage is developed across it which is proportional to the emitter (and hence collector) *current*. Current feedback increases the input impedance but does not affect the current gain of the stage.

WIDEBAND LINEAR R.F. AMPLIFIER

The ZTX320/BFW97 RF transistor can be used in a two transistor feedback pair circuit to provide a current amplifier of controlled gain and bandwidth. The circuit is shown in Fig. 9.5.

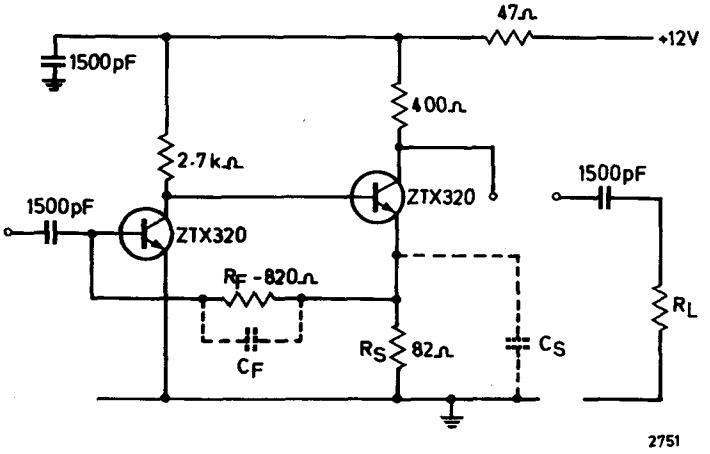


Figure 9.5

The current gain is given by the resistor ratio

$$\frac{R_F + R_S}{R_F} \simeq 10$$

The circuit exhibits a peak in the high frequency response curve, due to stray capacitances across the emitter and collector resistors. The addition of compensating capacitors C_F and C_S will give a level frequency response. Due to the high frequencies involved the components should be assembled closely together to reduce stray capacitance and lead inductance.

Typical performance for the above circuit was measured as follows:—

Gain = 10
Bandwidth at 3 dB down = 230 MHz
Current from 12V supply = 12mA
Compensation capacitors C_F = 1pF C_S = 2pF

The nature of the feedback gives a very low input impedance typically less than 10 ohms and the circuit was fed by the matching network shown in Figure 9.6.

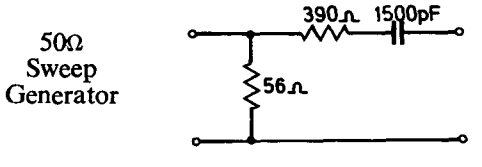


Figure 9.6

The 390Ω feed resistor gives an input resistance equal to the output resistance, and a comparison of input voltage across the 56Ω resistor and the output voltages can be taken as a direct measure of current gain.

The amplifier power consumption is typically 150mW at 12V. The standing currents of the transistors are 3mA and 10mA respectively. With a nominal 400Ω collector load the output voltage is 8V D.C. quiescent with a 12V supply. The maximum undistorted output is approximately 7 volts peak-to-peak with no load connected, falling to 0·5 volts peak-to-peak across a 50 ohm load.

Input Matching Stage

A grounded base ZTX320 can be used to provide an input of 50Ω to match standard 50Ω cables or sources. The input resistance of the grounded base transistor stage is given by

$$R_{IN} \simeq r_e \simeq \frac{25}{I_E\,(mA)}$$

By biasing the transistor to 0.5mA a reasonable match can be achieved. The complete circuit is shown in Fig. 9.7.

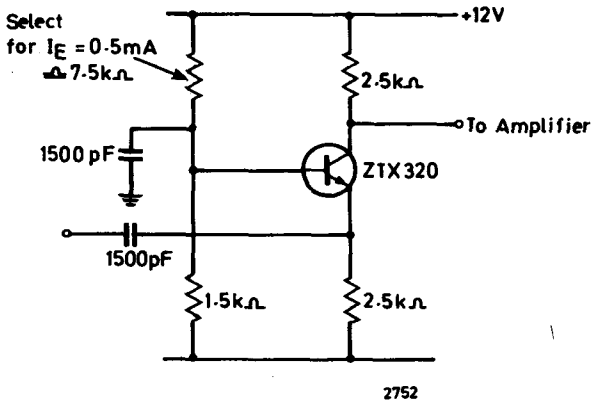


Figure 9.7

Typical performance was measured as

Overall gain (50Ω source, 50Ω load) = 9·2
3dB bandwidth = 250 MHz

The wide bandwidth of the basic circuit shown in Fig. 9.5 can be sacrificed, in exchange for increased current gain, by the use of alternative resistor ratios.

The following alternative circuits were built and the performances measured.

(a) R_F = 2·7kΩ R_S = 82Ω
Current gain = 25
3dB bandwidth = 130 MHz
Compensation Capacitors C_F = 0, C_S = 11pF.

(b) R_F = 4·7KΩ R_S = 82Ω
Current gain = 42
3dB bandwidth = 50 MHz
Compensation Capacitors C_F = 0, C_S = 22pF + (4-20pF trimmer).

As the frequency compensation required is dependent on circuit layout, the values of capacitors given are approximate. For optimum flatness of response a sweep generator and visual display should be used and the capacitors adjusted accordingly.

The low input impedance is a major advantage when stages are used in cascade. The inter-stage capacitance has little effect on the overall bandwidth.

WIDEBAND CURRENT AMPLIFIER

This circuit has a low input impedance and a relatively high output impedance, with a bandwidth of over 6MHz.

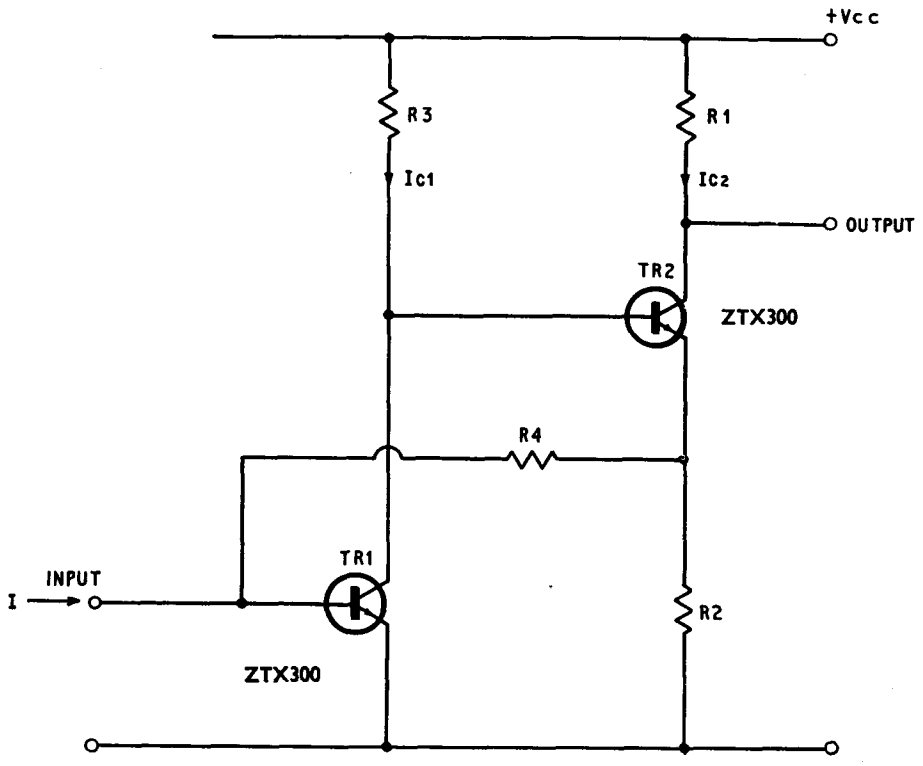


Figure 9.8

Design Procedure

(1) Choose supply voltage—say 12V (maximum 25V for ZTX300 or BCW10).

(2) Choose Tr2 collector current. For maximum f_T this should be between 3 and 20mA. For maximum transfer resistance

$$\text{i.e. } \frac{V_{out}}{I_{in}}$$

I_{c2} should be as small as possible to allow R_1 to be large. This will reduce bandwidth due to stray capacitance and fall in f_T, say $I_{c2} = 5mA$.

(3) Choose R_1 to drop about 1 volt less than half of the supply volts (to allow for the p.d. across R_2). Therefore $R_1 = 1k\Omega$.

(4) The emitter-base junction of Tr1 will have a p.d. of approximately 0·7 volts and R_4 will drop a further 0·1-0·2V. Therefore choose R_2 to drop 0·9V. Therefore $R_2 = 180\Omega$.

(5) Choose R_3 to be about five times R_1. Therefore $R_3 = 4{\cdot}7k\Omega$.

(6) Choose R_4 for current gain required.

Current gain $A_I \approx \frac{R_4}{R_2}$ (more accurately $\frac{R_4}{R_2} + 1$)

Therefore for current gain of 10 $R_4 \approx 1{\cdot}8k\Omega$
for current gain of 20 $R_4 \approx 3{\cdot}6k\Omega$

(*Note:* Maximum value of R_4 is that which will drop approximately 0·3V, i.e. 10kΩ with min. gain transistors in this case).

Final Circuit

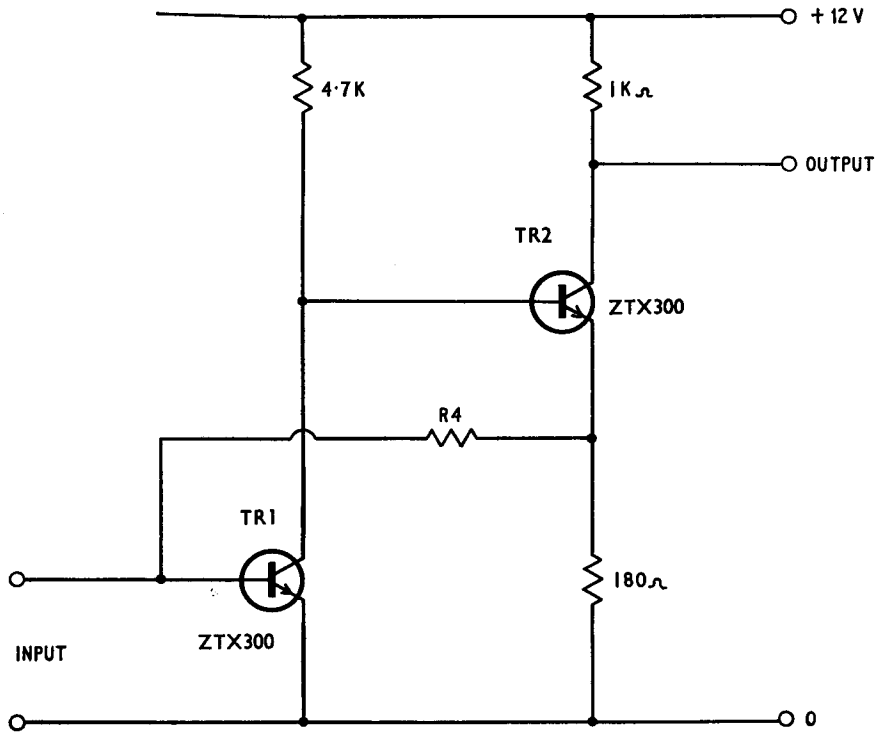


Figure 9.9

With R_4 = 1·8kΩ; bandwidth = 9MHz, current gain = 10.
= 3·6kΩ; bandwidth = 6·5MHz, current gain = 20.

Input impedance ≈ 15Ω.

Output impedance = 1kΩ.

Tr1, Tr2 ZTX300 (BCW10)

WIDEBAND VOLTAGE AMPLIFIER

An amplifier with a high input impedance, a low output impedance and a bandwidth of 14MHz.

(1) Choose supply voltage, say 10V.

(2) Choose Tr3 collector current. A value of 10mA will be used as an example as the current gain of the ZTX300 (BCW10) reaches a peak at this current.

(3) Choose $R_7 + R_2$ to drop half of the supply voltage, also the ratio $\frac{R_7 + R_2}{R_2}$ gives the voltage gain.

Thus $R_7 + R_2 = 500\Omega$ and for a gain of approximately 20, $R_7 = 470\Omega$, $R_2 = 22\Omega$.

(4) Choose R_6 as 5-10 times R_7. The higher value will give higher open loop gain and lower distortion, the lower value will give a greater bandwidth.

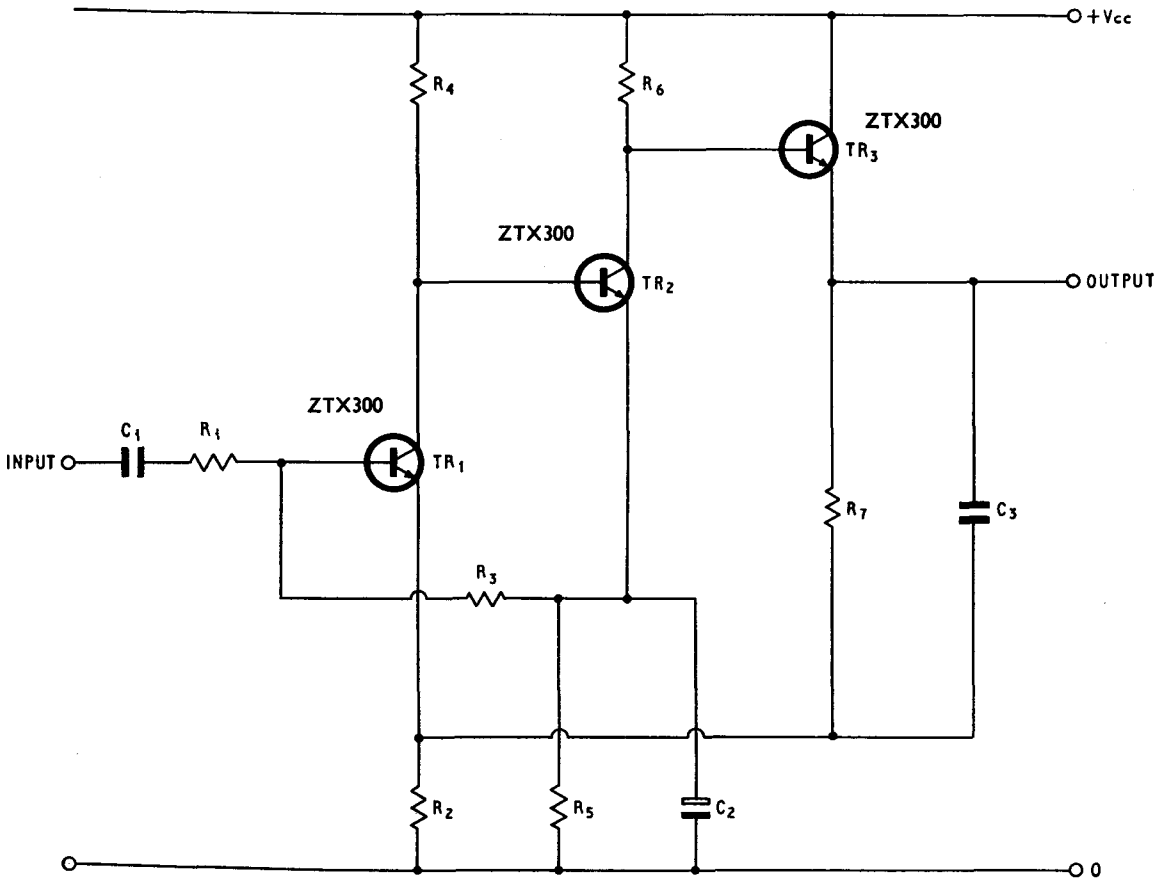
R_6 = 4·7k.

(5) Choose Tr2 collector current to drop half of the supply voltage across R_6, therefore I_{c2} = 1mA.

(6) Choose R_5 to drop approximately 1 volt.

p.d. across R_2 = 0·25V in this case
V_{be} of T_{R1} ≈ 0·6V } estimated
p.d. across R_3 ≈ 0·1V } values
0·95V

Therefore R_5 = 1kΩ.



Tr1, Tr2, Tr3—ZTX300 (BCW 10)

Figure 9.10

(7) Choose R_4 about 5 times R_6, therefore $R_4 = 22k\Omega$.

(8) Calculate collector current of Tr1 $= \dfrac{V_{cc} - 1{\cdot}7}{R_4}$

$= 380\mu A$

and hence the base current of Tr1 $= \dfrac{380\mu A}{h_{FE(min)}} = \dfrac{380}{30} \approx 13\mu A.$

(9) Choose R_3 to drop not more than 0·2V,
if $R_3 = 10k\Omega$, p.d. due to base current = 0·13V which is satisfactory.

(10) Choose capacitor values. For wideband amplification $C_2 > 50\mu F$, $C_1 > 10\mu F$.
C_3 is necessary to remove a peak in the frequency response at high frequencies. In this example a value of 15pF was found to give maximal flatness.

(11) R_1 is a parasitic stopper. A value of 470Ω was found to be adequate for the experimental circuit. With more careful construction it may not be necessary.

Final Circuit

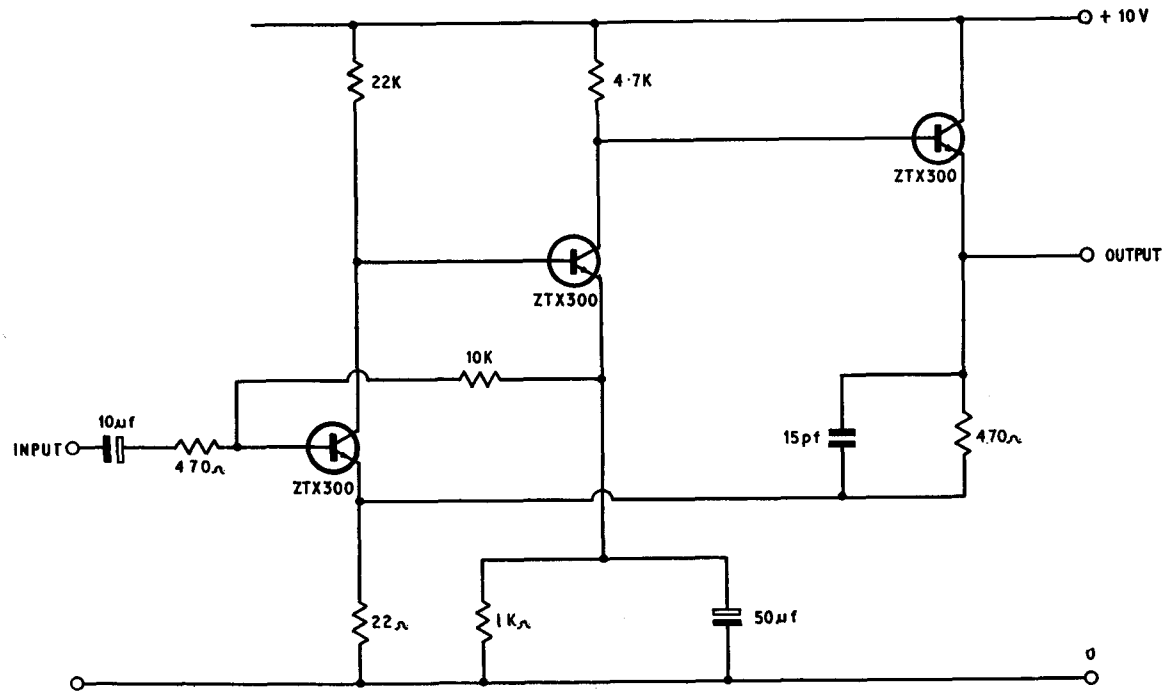
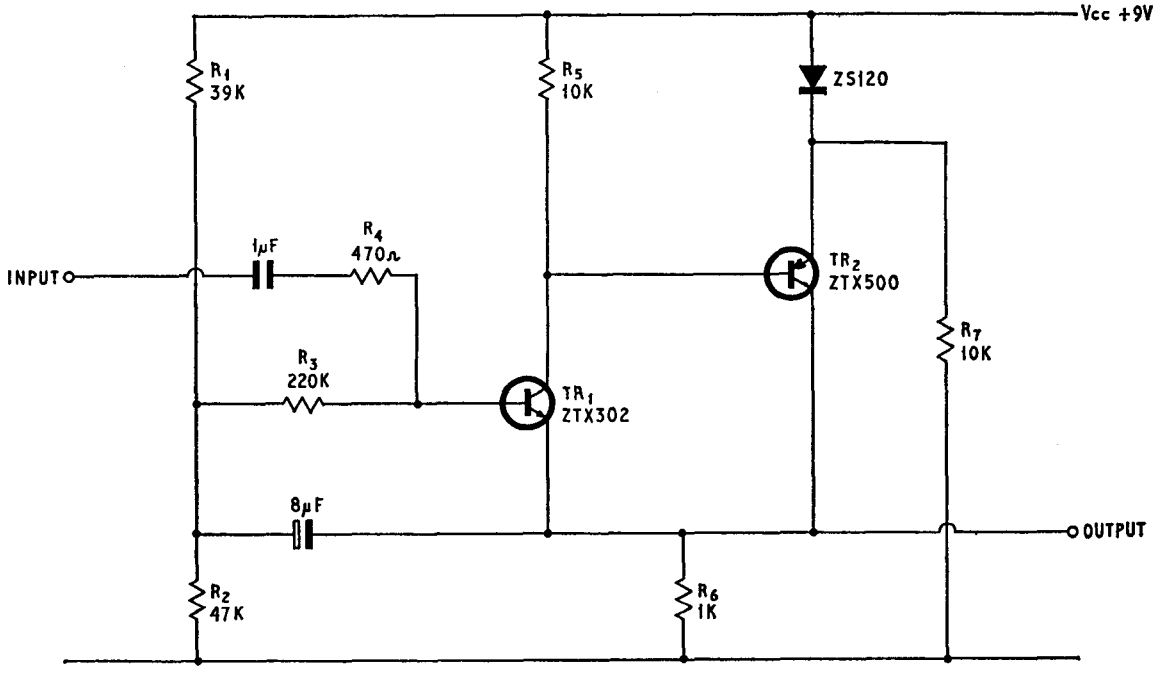


Figure 9.11

3dB bandwidth 14 MHz.
Voltage gain 20.
Input impedance ≈ 10kΩ.
Tr1, Tr2, Tr3 ZTX300 (BCW10)

HIGH IMPEDANCE, UNITY GAIN AMPLIFIER



Tr1—ZTX302 (BCW14)
Tr2—ZTX500 (BCW11)

Figure 9.12

(1) The value of R_6 is a compromise between input impedance and bandwidth. For the value shown (1kΩ) the input impedance is > 1MΩ and the bandwidth > 1MHz at 1V r.m.s. output. By increasing R_6 a higher input impedance can be obtained at the cost of reduced bandwidth.

(2) Tr2 operates at a collector current of 4mA, and to produce this collector current, a base current of 35μA is required (average).

(3) The bleed resistor R_5 takes 120μA, so the total current drawn from Tr1 = 155μA (average). Therefore Tr1 base current ≈ 2μA.

(4) This causes a volt drop of approximately 0·5 volt across R_3 and the effective resistance of the potential divider formed by R_1 and R_2.

(5) The values of R_1 and R_2 are not important, but the effective resistance of R_1 and R_2 in parallel should be large compared with R_6 and small compared with R_3. R_1 and R_2 are chosen to give a potential of 5 volts at the junction with R_3. This gives approximately 4 volts across R_6.

(6) **Performance**

This circuit has an input impedance of at least 1MΩ (depending on the current gain of the transistors used).

$$Z_{in} \approx (h_{fe1} \times h_{fe2} \times R_6).$$

Bandwidth is > 1MHz at 1 volt r.m.s. output. Bandwidth here means the frequency at which waveform distortion is just visible, not the -3dB point, which is at a higher frequency.

Voltage gain of the test circuit was 0·995. This can be increased to exactly unity by the modification shown in Figure 9.13. The value of R_8 depends on the current gains of the transistors used.

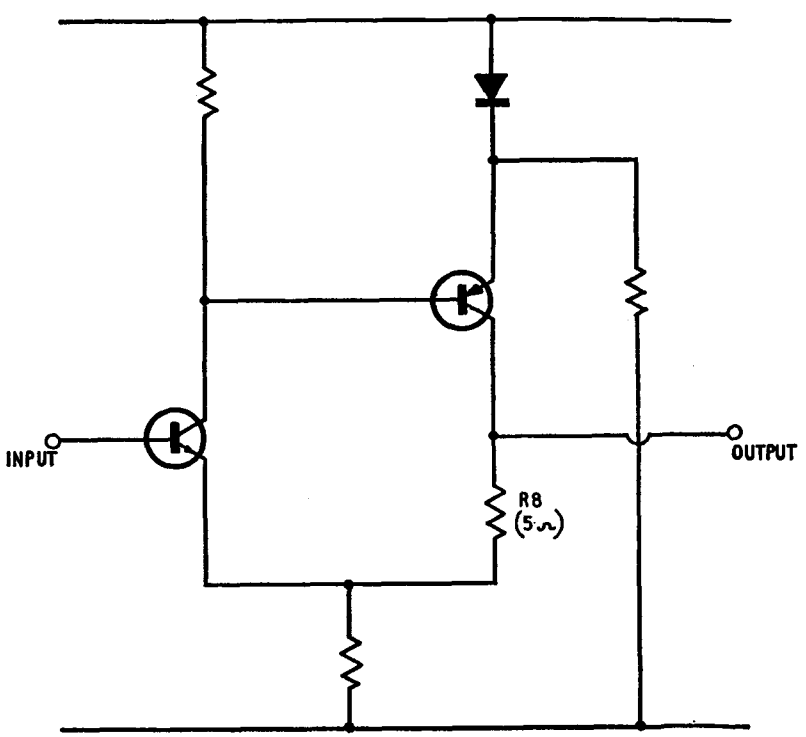


Figure 9.13

SECTION 10

MISCELLANEOUS CIRCUITS

A.C. MILLIVOLTMETER, RECTIFIER STAGE

This circuit will give full scale deflection on a 100μA linear scale meter for an input of approximately 20mV r.m.s. over a bandwidth of 800 kHz.

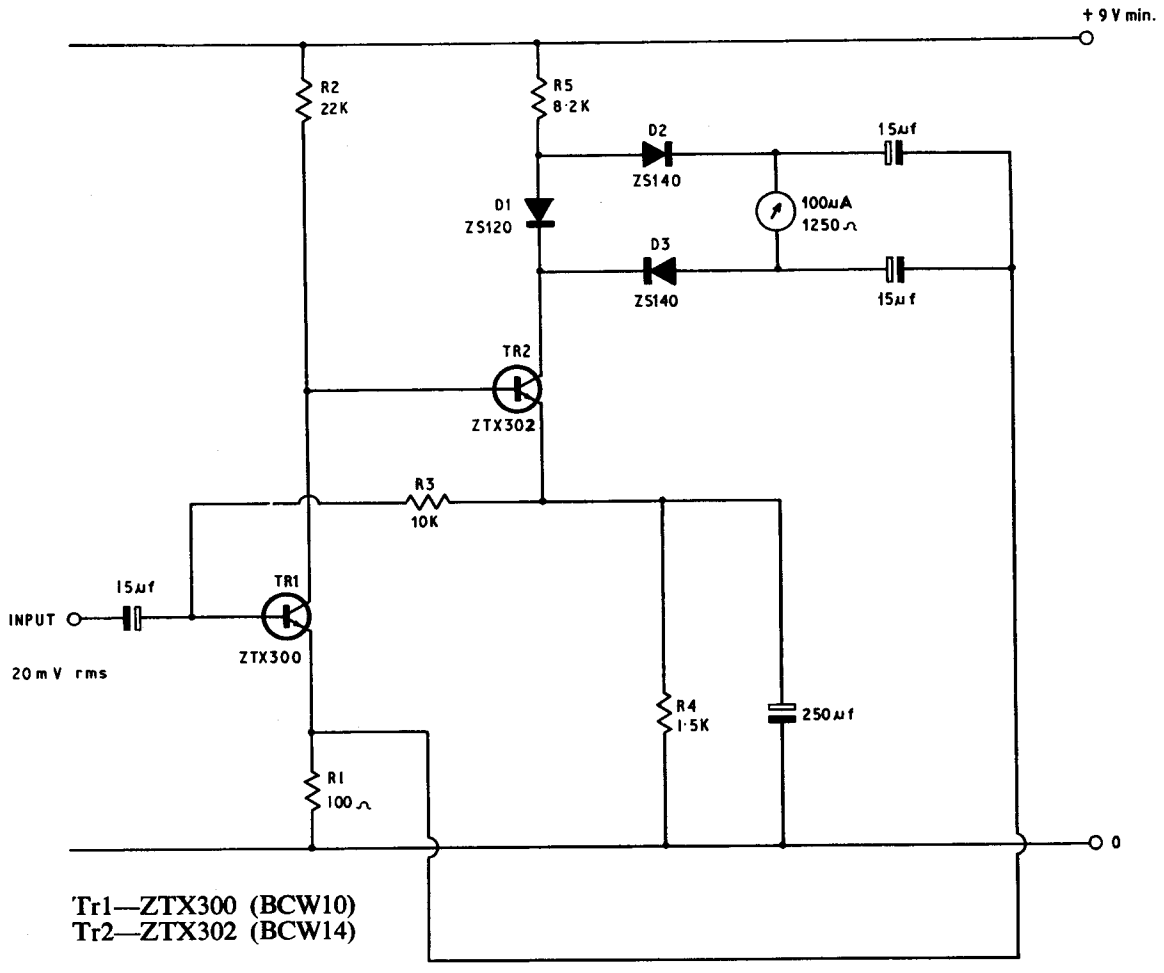


Figure 10.1

(1) The type of rectifier bridge shown requires an input of 220μA r.m.s. (310μA pk.) for full scale deflection of a 100μA meter. Tr2 is therefore biased at a collector current of 0·5mA to ensure that adequate output current is available.

(2) R_5 is chosen to drop slightly less than half the supply voltage (to allow for the p.d. across D_1). 8·2kΩ is suitable.

(3) R_4 is chosen to drop approximately 0·8V. Therefore R_4 = 1·5kΩ.

(4) Tr1 collector current is a compromise between input impedance and open loop gain (and hence linearity). There is, however, no advantage in using a collector current greater than about 0·5mA since the r_e of the transistor is then falling below the external emitter resistance R_1 (100Ω). A bias of 340μA is used in this design.

(5) R_3 is chosen to drop about 0·1V. Tr1 requires approximately 10μA base current, so R_3 = 10kΩ.

(6) A flat response down to about 10Hz is usually required, so large value coupling and decoupling capacitors are necessary. The values shown in the circuit have been found adequate.

Performance

Sensitivity 22mV for f.s.d. (can be adjusted by variation of R_1).

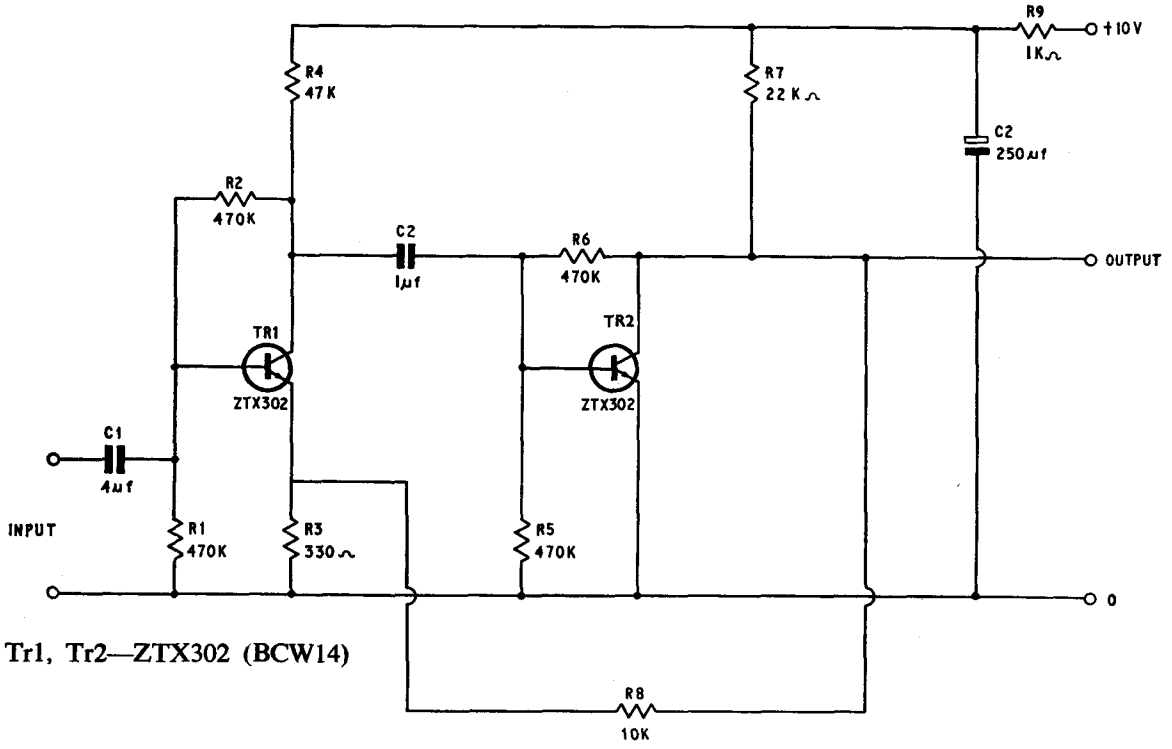
Bandwidth 10Hz – 800kHz +0 – 5%.

Input impedance = 10kΩ.

No non-linearity detectable by comparison with Solartron VM1484 true r.m.s. voltmeter.

MILLIVOLTMETER PRE-AMPLIFIER

This circuit will increase the sensitivity of the rectifier stage already described to 1mV f.s.d.



Tr1, Tr2—ZTX302 (BCW14)

Figure 10.2

(1) To achieve maximum voltage gain Tr2 load resistance should be as high as possible. Consequently Tr2 is operated at a low collector current ($\approx$ 300μA), and a 22kΩ d.c. load is used.

(2) The base current for Tr2 is derived from R_6 and R_7, the average current gain of ZTX302 at 300μA $\approx$ 100

Therefore base current = 3·0μA

Current through R_5 $\approx$ 1·3μA

Therefore for collector-base voltage of 2·0V (V_{ce} = 2·6V)

$$R_6 = \frac{2}{4{\cdot}3\mu A} = 470k\Omega.$$

R_5 reduces the effect of transistor gain spread on the bias and reduces the recovery time of the stage to a large overload.

(3) For minimum noise Tr1 is operated at a very low collector current ($\approx$ 100μA). It is biased in the same way as Tr2.

(4) The input impedance is approximately 40kΩ without feedback, when the feedback is connected the input impedance becomes greater than 100kΩ. R_3 is adjusted to give the voltage gain required. For a gain of 22 its value is approximately 330Ω.

(5) To avoid the possibility of L.F. oscillation with a battery supply the pre-amplifier is heavily decoupled by R_9 (1kΩ) and C_3 (250μF).

Performance

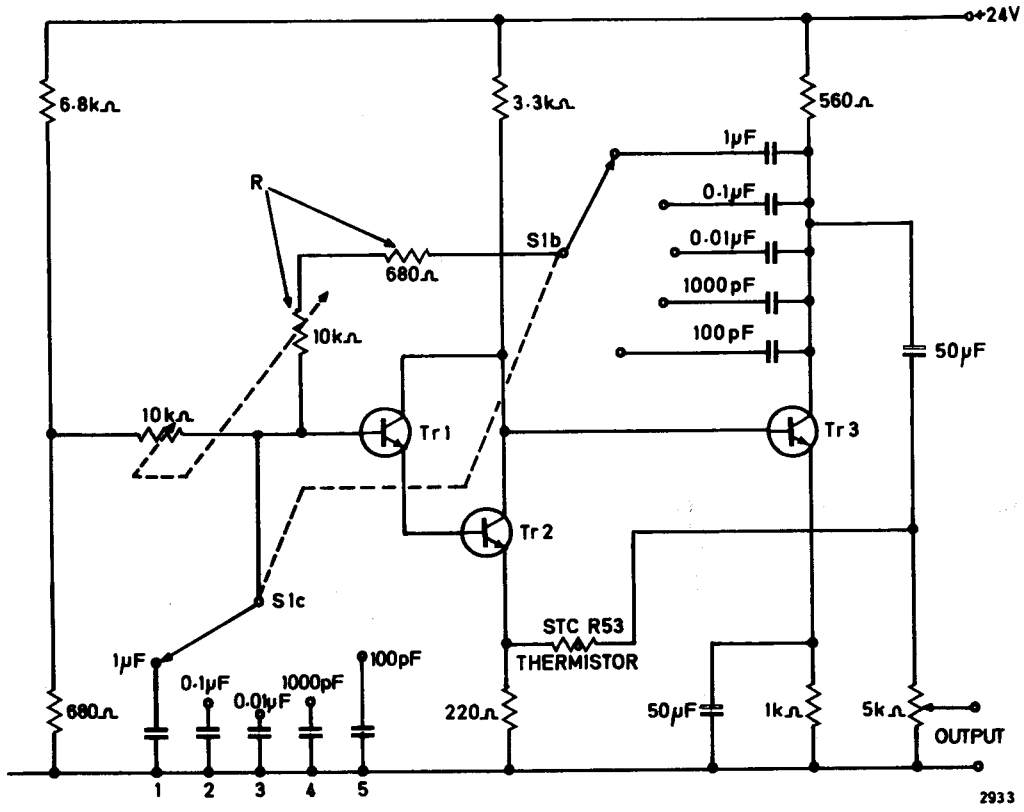
Bandwidth (used with rectifier stage) = 800kHz +0 −5%.

Noise with 1kΩ source <5μV

Voltage gain = 22 (adjustable).

Input impedance = 100kΩ.

WIDE-RANGE WIEN BRIDGE OSCILLATOR



Tr1, Tr2, Tr3 ZT300 (BCW10) Figure 10.3

This oscillator will operate over a wide frequency range, from less than 10Hz to 5MHz. The output is 1 volt r.m.s. with less than 0·2% total harmonic distortion (at 1kHz). The circuit shown above has five ranges:

(1) 15Hz – 200Hz
(2) 150Hz – 2kHz
(3) 1·5kHz – 20kHz
(4) 15kHz – 200kHz
(5) 150kHz – 2MHz

The frequency of oscillation is given by $fo = \frac{1}{2\pi RC}$

VERY LOW DISTORTION WIEN BRIDGE OSCILLATOR

This circuit (Figure 10.4) gives a very low distortion output over a restricted frequency range. It is primarily intended to enable distortion measurements to be made on audio amplifiers, without the inconvenience of tuned filters.

Design

(1) At 1V r.m.s. output (normal level for R53 thermistor) the worst case load on Tr3 is approximately 200Ω. (R_{11} in parallel with 4·7kΩ, and 600Ω plus thermistor and Wien network).

Therefore peak a.c. current in Tr3 $= \frac{\sqrt{2}}{200} = 7{\cdot}07\text{mA}$

so Tr3 is biased at 10mA to provide adequate drive under all conditions.

(2) R_{11} is chosen to drop half of the supply voltage, 1kΩ is suitable.

(3) R_{10} is chosen as five times R_{11} = 4·7kΩ.

(4) R_9 is chosen as half of R_{10} = 2·2kΩ.

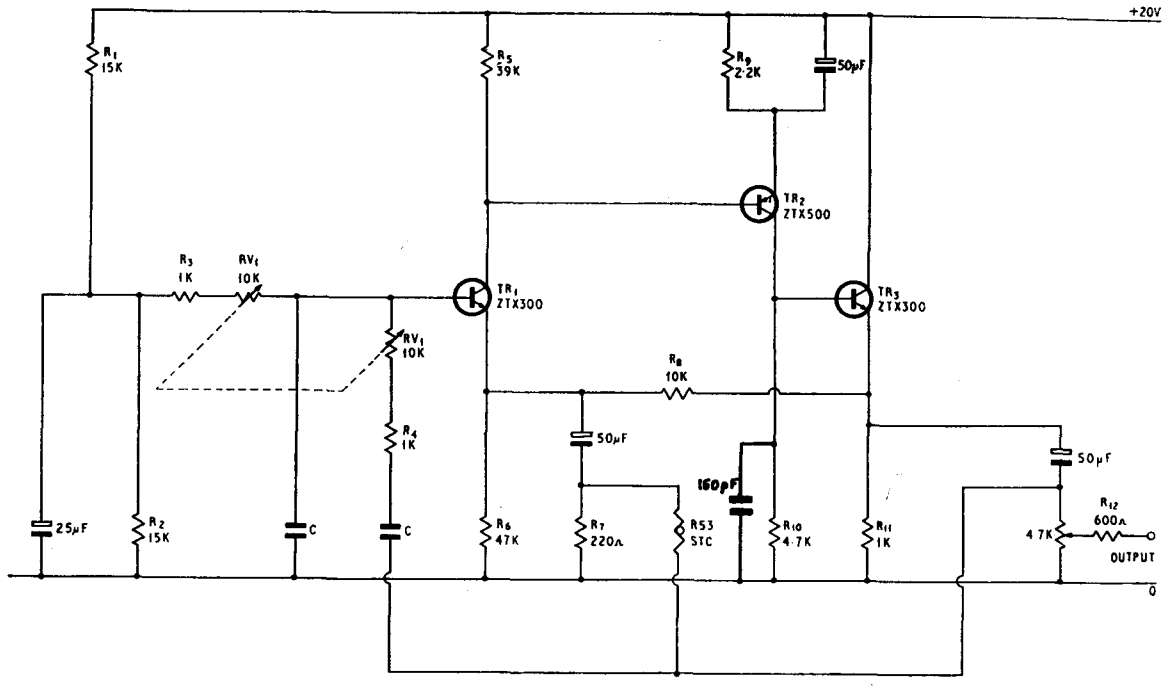


Figure 10.4

(5) Tr2 collector current is chosen to drop half of the supply volts + 0·7V (V_{be} of Tr3) across R_{10}

$$I_{c2} = \left(\frac{10{\cdot}7}{4{\cdot}7} + 0{\cdot}1\right) \text{mA}$$

(0·1 mA: base current of Tr3)

$= 2{\cdot}4\text{mA}.$

Therefore p.d. across $R_9 \approx 2{\cdot}4 \times 2{\cdot}2 = 5{\cdot}3$ volts.

Max. base current required by Tr2 $\approx 55\mu\text{A}$.

(6) For lowest noise, and to achieve a high input impedance, Tr1 is operated at a low collector current (213μA).

$$\text{Thus the value of } R_5 = \frac{\text{Volt drop across } R_9 + V_{be} \text{ of Tr2}}{I_c \text{ of Tr1} - I_b \text{ of Tr2}}$$

$$= \frac{5{\cdot}3 + 0{\cdot}7}{213 - 55} \times 10^6\Omega$$

$$= 39\text{k}\Omega.$$

R_6 has half of the supply volts dropped across it, and hence its value $= \frac{10}{0{\cdot}213}\ \text{k}\Omega \approx 47\text{k}\Omega$.

(7) R_1 and R_2 are chosen to bias Tr1 at half of the supply voltage. Their exact value is unimportant; values of 10-22kΩ are suitable.

(8) The exact value of R_8 is again unimportant but it should be large compared with R_{11} and small compared with R_6. A value of 10kΩ is suitable.

(9) R_7 is chosen as 220Ω to give the correct operating conditions for the thermistor.

(10) RV_1 is chosen so that its maximum value is very much less than the input impedance of Tr1 ($\approx$ 1MΩ). A value of 10kΩ is suitable.

(11) R_3, R_4 are chosen to give the frequency ratio covered on each range. 1kΩ gives a max. to min. ratio of 11 : 1 giving a small overlap on decade ranges. If a more open frequency scale is required R_3, R_4 can be increased to 3·3kΩ giving 4 : 1 coverage on each range.

(12) The capacitors required for each range are calculated from the formula $C = \frac{1}{2\pi f_o R}$ where $R = RV_1 + R_3$.

f_o = lowest frequency on each range.

Performance

Frequency range < 10Hz to 100kHz.
Harmonic distortion < 0·01% at 1kHz [·004% measured].
Output $\approx$ 1·0V r.m.s.
Output impedance $\approx$ 600Ω.

PROCESS TIMER

This circuit will hold a relay on for a period variable between one and ten seconds. The action is initiated by a negative input pulse, which may be derived from other circuitry or from a simple switch.

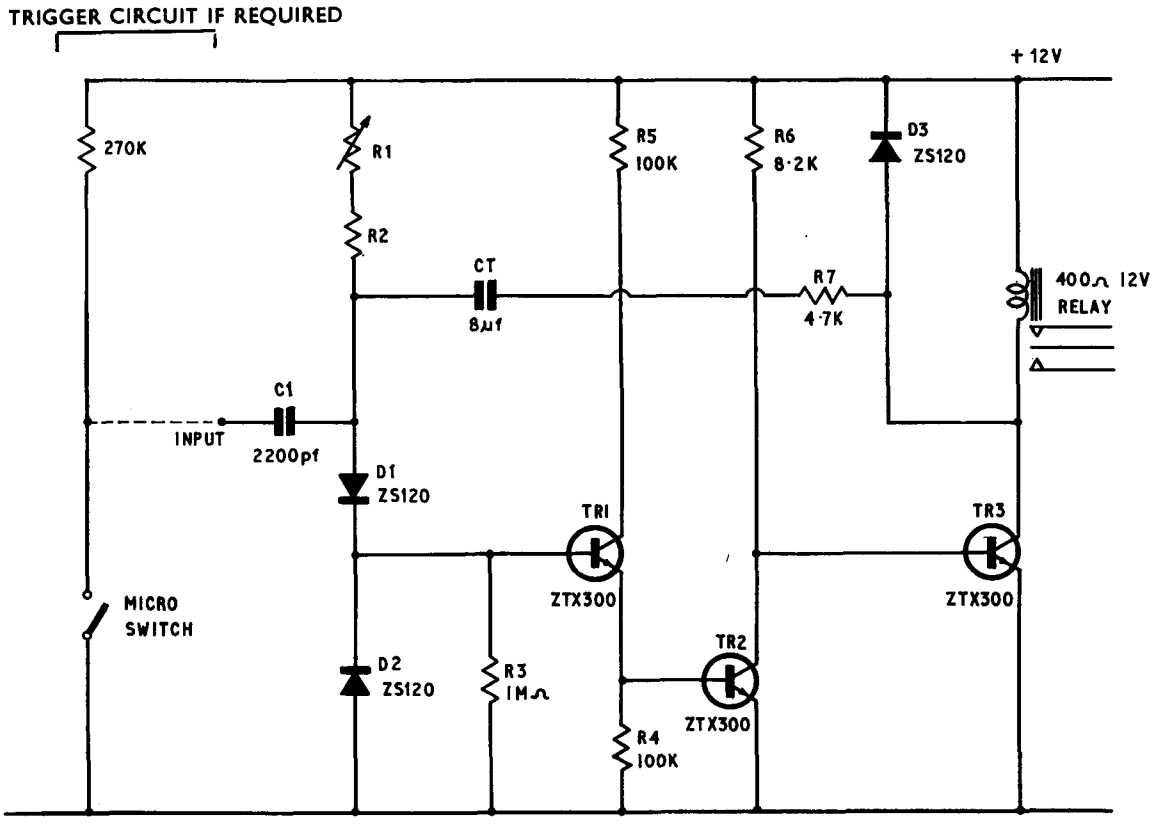


Figure 10.5

(1) The circuit was designed to operate a 12V 400Ω relay. If the relay coil resistance has a tolerance of ±20% then the maximum current required $= \frac{12}{400 \times 0{\cdot}8} = 37{\cdot}5\text{mA}$.

At this current, the current gain of a ZTX300 (BCW10) is 86% of the 10mA value. Also to ensure satisfactory operation at temperatures down to -10°C a further 25% fall in gain must be allowed for.

Therefore, worst case current gain of Tr3 $= 50 \times 0{\cdot}86 \times 0{\cdot}75$
$= 32{\cdot}2.$

(2) Maximum base current required by Tr3 $= \frac{37{\cdot}5\text{mA}}{32{\cdot}2} = 1{\cdot}16\text{mA}.$

The maximum value of R_6 is given by $\frac{V_{cc} - V_{be}\,(Tr3)}{I_b\,(Tr3)}$

$$R_6 \text{ max.} = \frac{12 - 0{\cdot}7}{1{\cdot}16} = 9{\cdot}75\text{k}\Omega$$

Allowing a ±20% life tolerance for R_6 the nominal value is

$$R_6 \text{ nom.} = \frac{9{\cdot}75}{1{\cdot}2}\text{k} = 8{\cdot}12\text{k}\Omega$$

Therefore $R_6 = 8{\cdot}2\text{k}\Omega$.

(3) The minimum value of $R_6 = 8{\cdot}2k \times 0{\cdot}8 = 6{\cdot}56k\Omega$.

Therefore the maximum current drawn from Tr2 $= \frac{V_{cc}}{R_{6(min)}} = \frac{12}{6{\cdot}56}mA = 1{\cdot}83mA$.

At this collector current the current gain of a ZTX300 is 80% of the 10mA value, and operation at –10°C results in a further 25% reduction.

Tr2 $h_{FE(min)} = 50 \times 0{\cdot}8 \times 0{\cdot}75 = 30$.

(4) The base current required by Tr2 under worst conditions

$$I_{b(TR2)} = \frac{1{\cdot}83mA}{30} = 61\mu A.$$

(5) The bleed resistor R_4 takes a nominal current of $7\mu A$, which is five times greater than the collector-base leakage current (I_{cbo}) of Tr2 at + 55°C. With R_4 20% low, this current increases to $9\mu A$.

Therefore, max. current that Tr1 needs to supply = 61 + 9 = $70\mu A$.

(6) At $70\mu A$ the current gain of Tr1 (ZTX300) is 43% of the 10mA value and –10°C operation reduces this a further 25%.

Therefore h_{FE} (Tr1) = $50 \times 0{\cdot}43 \times 0{\cdot}75 = 16{\cdot}1$.

The base current required by Tr1 $= \frac{70\mu A}{16{\cdot}1} \approx 4{\cdot}3\mu A$.

P.d. across D_1 and Tr1 and Tr2 bases $\approx$ 2·1 volts.

The maximum value of $(R_1 + R_2) = \frac{12 - 2{\cdot}1}{4{\cdot}3}\ M\Omega$

$= 2{\cdot}3M\Omega$.

(7) Under quiescent conditions the anode of D_1 rests at approximately +2·0 volts and the collector of Tr3 at +12 volts. When the circuit is triggered, Tr3 collector voltage falls to (approximately) zero. This change is transmitted through the timing capacitor C_T, driving D_1 anode to –10 volts. C_T now starts to charge from –10 volts towards +12 volts. However, when C_T has charged to +2 volts, D_1 and Tr1 and Tr2 start to conduct and the circuit reverts to its quiescent state. The monostable period is found as follows:

$$\left[2 - (-10)\right] = \left[12 - (-10)\right] \times \left[1 - e^{-\frac{t}{CR}}\right]$$

$$\frac{12}{22} = 1 - e^{-\frac{t}{CR}} \quad , \therefore e^{-\frac{t}{CR}} = \frac{10}{22}$$

$$\frac{t}{CR} = 0{\cdot}787.$$

Therefore the monostable period is given by multiplying the time constant $C_T \times (R_1 + R_2)$ by 0·787.

For a timing range of 1-10 seconds, a timing capacitor of $8\mu F$ is convenient and gives

$R_2 = 200k\Omega$

$R_1 = 2M\Omega$ pot.

(8) The purpose of the diodes D_1, D_2 is to protect Tr1 and Tr2 from the 12V negative transient when Tr3 turns on. D_3 absorbs the inductive spike produced by the relay coil when Tr3 turns off. R_7 was found necessary to prevent the circuit from free-running due to the relay coil "ringing". R_5 (100kΩ) limits the current flowing in Tr1 and Tr2 base to $100\mu A$.

THE USE OF THE BASE EMITTER JUNCTION OF THE ZTX300 AS A ZENER DIODE

Histograms of breakdown voltages of reversed biased base emitter junctions with two values of reverse currents are shown in Figures 10.6 and 10.7. The typical breakdown voltage is 8 volts and the devices exhibit a hard characteristic.

Slope impedance at 20mA is typically 20Ω and maximum dissipation is 200mW.

Temperature coefficient is +5·45 mV/°C or +0·059%/°C.

A sample batch of ZTX310 (BSV23) transistors had typical breakdown voltages in the 6-7·5V region with similar slope resistance to the ZTX300 (BCW10).

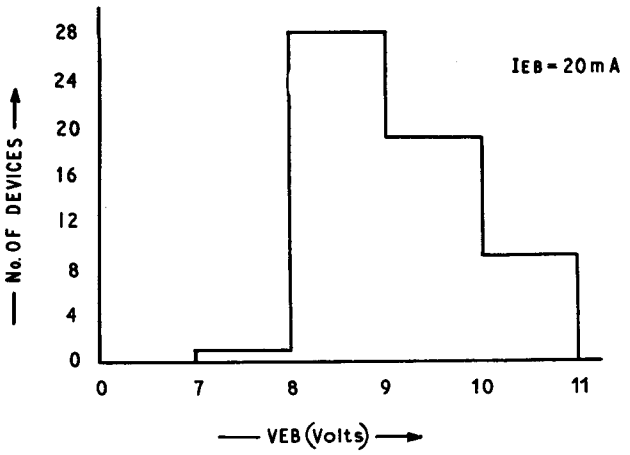


Figure 10.6

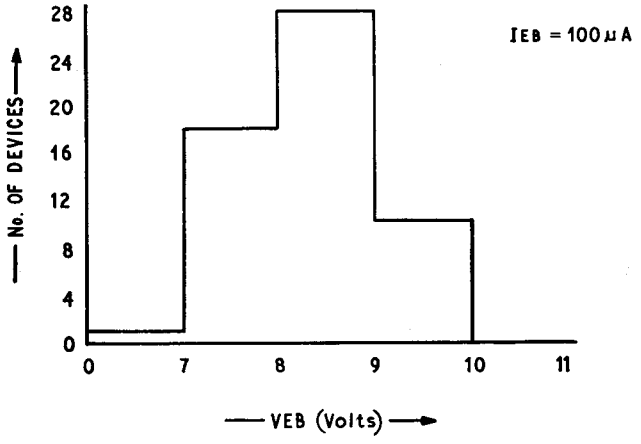


Figure 10.7

Degradation of D.C. Current Gain during Breakdown of Emitter Base Junction.

The emitter base junction of an E-line transistor may be used satisfactorily as a zener diode as stated above. If however the device is required to act both as a zener diode and as a transistor, it should be noted that a marked decrease in D.C. current gain may result.

The degradation of current gain is dependen on the amplitude and duration of the avalanche current and the surface condition of the particula transistor. It is attributed to high energy electrons, liberated by avalanche multiplication, colliding with silicon atoms at the silicon–silicon dioxide interface. The effect is to produce additional surface states, within or near the depletion layer, causing a reduction in current gain. The degree of degradation is difficult to predict as it depends on the avalanche current, the ionic charge in the oxide, (which is dependent on processing), the surface state of the transistor, again process dependent, and the transistor geometry.

USING THE ZTX300 (BCW10) AS A DIODE

Three possible methods of connection are described:—

1. Collector/Base (with emitter connected to base).
   This connection gives a diode with a medium recovery time, small capacitance, and high reverse voltage determined by the collector-base junction.
2. Base/Emitter (collector connected to base).
   The diode has a short recovery time, small capacitance, and a low reverse voltage determined by the base-emitter junction.
3. Base/Emitter (collector connected to emitter).
   The diode has a long reverse recovery time, a large capacitance, and a low reverse voltage determined by the base emitter junction.

Typical Recovery Time and Capacitance

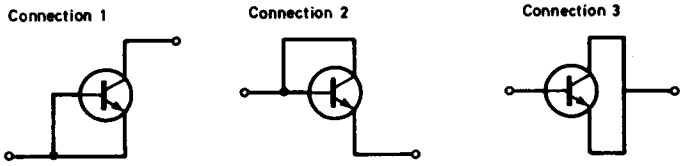


Figure 10.8

Method of Connection	Recovery Time nSec. $I_F=I_R=10mA$. $R=50\Omega$	Capacitance pF		
		at zero voltage	at reverse voltage	
			-10V	-5V
1	89	7	3	
2	2·7	7		3·5
3	244	13		5·5

The recovery time quoted is the interval between the negative input pulse attaining 10% of its final value and the reverse current attaining 10% of its maximum value.

The graph (Figure 10.9) shows the variation of capacitance with reverse voltage.

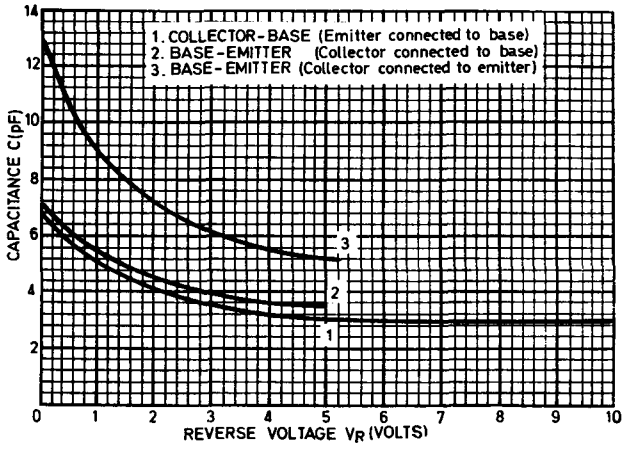


Figure 10.9

Junction Temperature Measurements ZTX300 (BCW10)

The maximum power dissipation of the ZTX300 in free air at 25°C is 300mW.

The thermal resistance, junction to ambient, θ_{JA} = 0·33°C/mW. Mounted on a Redpoint heat sink type 92.DC* the thermal resistance is reduced to θ_{JA} = 0·21°C/mW enabling 480mW to be dissipated at 25°C ambient.

With two transistors mounted in the same Redpoint heat sink, the heat sink should be clamped to a small aluminium plate to enable a worthwhile increase in power dissipation to be achieved. When clamped to an aluminium plate $1\frac{1}{2}'' \times 1'' \times$18swg, 480mW can be dissipated in each transistor.

If the transistor is clamped directly to a $1'' \times 1'' \times$ 18swg aluminium plate, a further reduction in thermal resistance occurs so that θ_{JA} = 0·17°C/mW, enabling 600mW to be dissipated.

The improved dissipation is offset, in some circumstances, by the fall of h_{FE} at higher collector currents. A higher drive power becomes necessary and it may well be more economic to operate output transistors in parallel, to achieve a given output power, than to use a heat sink and more powerful drive circuits.

*Redpoint Limited, Stratton St. Margaret, Swindon, Wilts.

STABLE VOLTAGE REFERENCE SOURCE

A ring of two reference circuit has been described* which provides two identical or dissimilar reference voltages. The circuit is shown in Figure 10.10.

The ZTX303 (BCW16) transistors are connected as diodes, the reverse biased based emitter junction acting as a zener diode. This reference source stabilises the base emitter potential of a transistor causing a constant collector current. The current flowing across a second reverse biased junction stabilises the base emitter voltage of the second transistor, whose collector current is the constant current source for the first simulated zener diode, completing the ring. It will be seen that two reference sources are available. The permitted range of supply voltage varies from the base collector breakdown voltage of the transistor (ZTX300 V_{CBO} 25V) to a minimum voltage given by:—

V supply min. $\geqslant V_{Z2} + V_{C1(sat)} + (V_{Z1} - V_{BE1})$.

Where V_{Z1} and V_{Z2} are the base emitter breakdown voltages, $V_{C1(sat)}$ is the saturation voltage of the first transistor and $V_{Z1} - V_{BE1}$ is the voltage across resistor R_1.

With the circuit shown, $V_{Z1} \simeq V_{Z2} \simeq 8V$, V_{C1} is typically 0·2V, and V_{BE} is typically 0·8V.

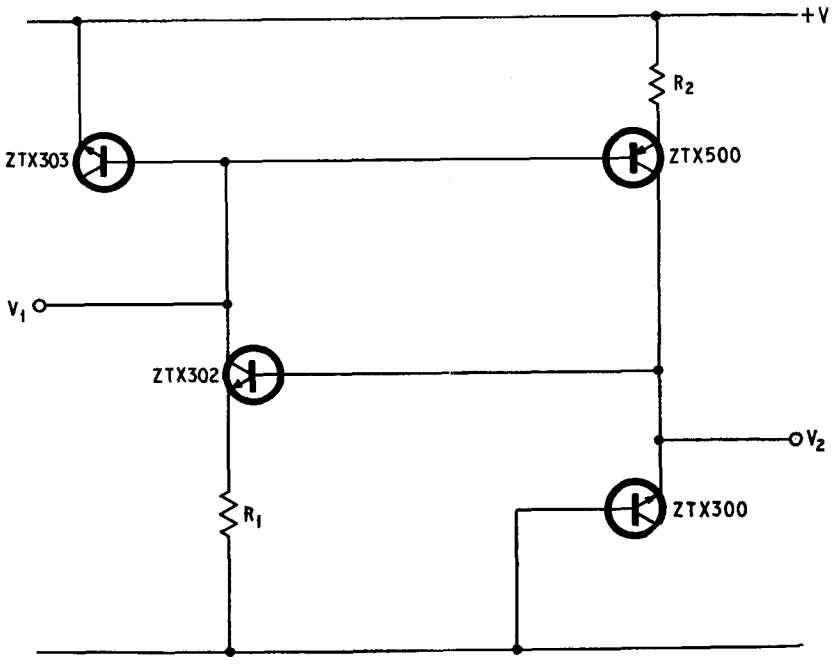


Figure 10.10

The transistor will saturate with a supply voltage of 8 + 0·2 + (8–0·8) = 15·4V.

The minimum supply voltage must therefore be above this value.

The Stabilisation Ratio ($S = \Delta V_{in}/\Delta V_{out}$) was measured, for a range of supply voltages, with R_1 and R_2 selected to give 1mA collector current in each transistor ($R_1 \simeq R_2 \simeq 6{\cdot}8k\Omega$).

The results are tabled below.

Supply Voltage	V_{out1} (via a 3·2 : 1 probe)	Stabilisation Ratio S
11·0	1·6507	—
12·0	1·7888	—
13·0	1·9065	—
14·0	2·1066	—
15·0	2·1088	100,000 : 1
20·0	2·1088	
25·0	2·1088	

Dissimilar collector currents had an adverse effect on the stability.

As the supply current is the sum of the collector currents, the circuit may be considered as a two terminal device using the supply terminals, when it can be used as a constant current source. For a typical line current of 2·5mA, a change of applied voltage of 5 volts will produce a current change of 3μA or 0·1%.

*"Ring of Two Reference", P. Williams, "Wireless World", July 1967.

D.C. AMPLIFIER

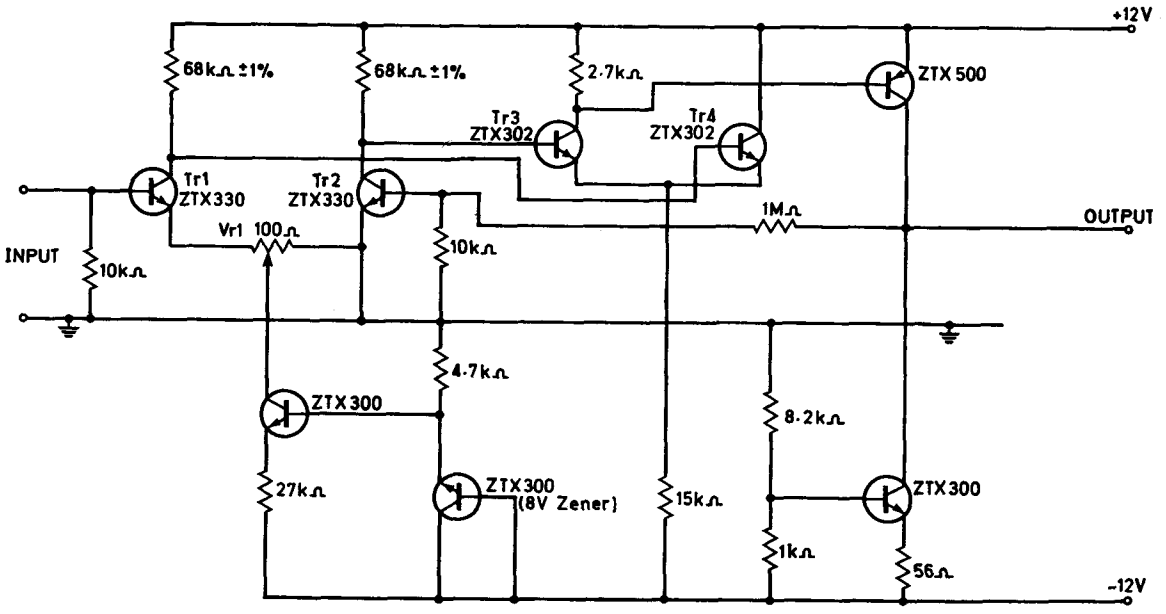


Figure 10.11

All resistors are ±10% unless otherwise stated.

Tr1 and Tr2 are a matched pair of ZTX330 (BCW20) transistors ($h_{FE1} = h_{FE2}$ ±10% at I_C = 100 μA), both transistors are held together in a "DELTA"* Model 203 heat sink, or mounted in a Redpoint heatsink, in order to maintain them both at a common ambient temperature. Tr3 and Tr4 are matched ZTX302's (BCW14) also held together in a similar manner. Potentiometer VR1 sets the output to zero voltage for zero input.

Typical Performance of Amplifier:

Maximum output voltage	±11V at ±10mA
Minimum load for full voltage swing	1·1kΩ
Nominal voltage gain	100
Bandwidth (3dB)	800kHz
Noise referred to input	<200μV peak-to-peak
Input impedance	10kΩ
Temperature drift	Approximately 25μV/°C referred to the input

The circuit must be shielded from draughts to prevent a temperature differential arising between Tr1 and Tr2 which could give rise to a large drift of output voltage.

*"DELTA" heat sink, model 203 (TO-18) obtainable from Jermyn Industries.

A CHOPPER D.C. AMPLIFIER USING ZTX330 (BCW20) TRANSISTORS

An alternative method of D.C. amplification is to chop the applied D.C. signal to produce a square wave of amplitude corresponding to the D.C. level. This can then be amplified in an A.C. amplifier which may have a large gain but has no D.C. drift problems. The output of the amplifier is fed to a demodulator which restores the signal to its D.C. component again. The chopper and demodulator are usually synchronised.

The ZTX330 (BCW20) transistor has a very low offset voltage when operating in the inverse mode, i.e. collector and emitter reversed. The typical value of the offset voltage developed across a 1·5kΩ load for a base input current of 500μA is about 0·25mV. Typical slope resistance for a base input current of 500μA is 10Ω for both positive and negative inputs.

The base-emitter reverse leakage current was found to be less than 20nA for all samples tested. These figures were obtained from several samples of ZTX330 and are reproduced here for guidance only. No guarantee can be given that any transistor supplied will conform to these measurements.

The Shunt Chopper

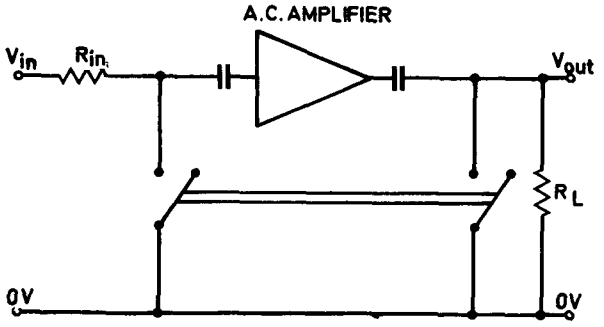


Figure 10.12

The voltage to be amplified is modulated by the chopper and the resultant square wave is amplified and then synchronously demodulated to give a d.c. output with the same polarity as that at the input.

Single Transistor Chopper

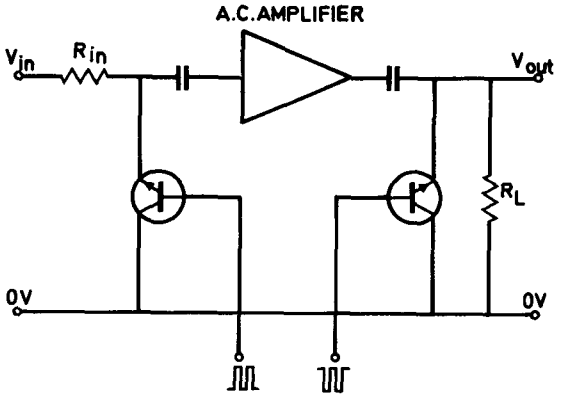


Figure 10.13

For good linearity, $V_{in} >>$ offset voltage of transistor, i.e. $V_{in} > 10mV$ for reasonable linearity.

Balanced Chopper Amplifier—Microvolt/Microamp Meter

The chopper transistor offset voltage can be balanced out with that of another similar transistor and voltages below 100μV can be measured accurately. In addition, when used in a balanced circuit, temperature drift is reduced as both transistors drift together.

Figure 10.14 illustrates a typical application using this principle.

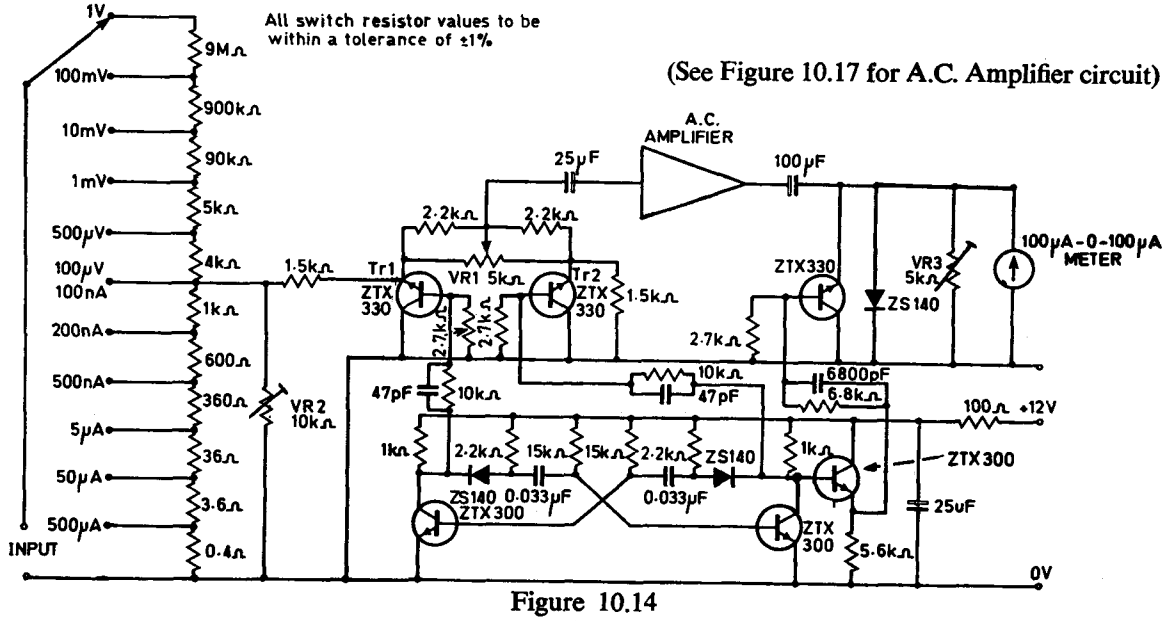


Figure 10.14

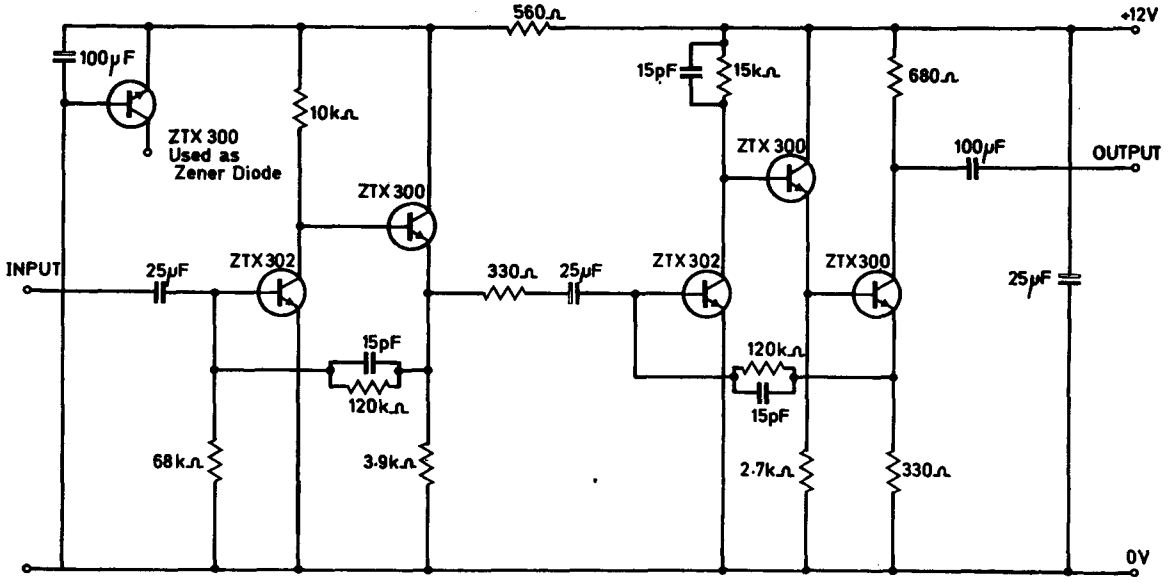


Figure 10.15—The circuit of the A.C. Amplifier portion of the Chopper Amplifier shown in Figure 10.14.

Setting-up

Adjust VR1 to give zero reading on the meter when the switch is in the 1 volt position and with zero input.

With the range switch at 100μV and VR2 at approximately mid position, feed in 100μV from a source of less than 10Ω impedance and adjust VR3 for full-scale deflection.

Adjust VR2 until full-scale deflection is also obtained for an input of 1V with the range switch in the 1V position.

For accuracy on the 100μV/100nA range, the source resistance must be less than 100Ω.

The meter used should be a 100μA-0-100μA centre zero moving coil type, with an internal resistance of less than 1kΩ.

Due to the high sensitivity of the A.C. amplifier, the whole unit, excluding power supply, should be enclosed in a metal box earthed to the circuit at the input only. The metal box will also screen Tr1 and Tr2 from draughts and improve the short term temperature stability of the amplifier.

All wiring must be as short as possible.

A low ripple power supply must be used and a suitable circuit is given in Figure 10.16. Output is set to 12V by adjusting VR1.

Ripple is approximately 15mV peak-to-peak.

Power Supply

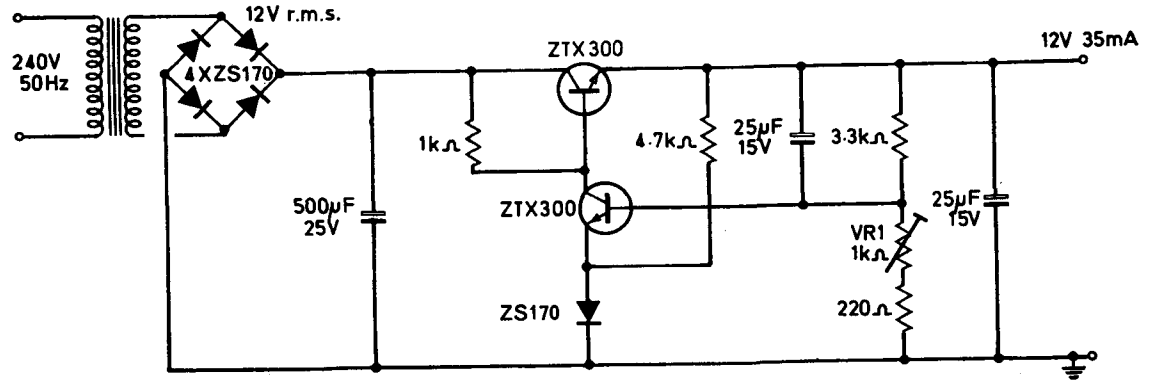


Figure 10.16

Specification

Supply voltage 12V at approximately 35mA. (Initial current upon switching on is considerably higher than this for a few seconds, due to the long time constants involved).

A.C. amplifier	Power gain 86dB typical Bandwidth 20Hz to 150kHz (–3dB) Noise $< 10\mu V$ peak-to-peak referred to input.
Chopping frequency	1·5kHz approx.
Input impedance on voltage ranges	10MΩ/volt
Voltage drop on current ranges	$\leqslant 200\mu V$
Linearity, excluding meter, is better than	3%

The final accuracy of the instrument will depend upon the accuracy with which the initial adjustments were made.

Temperature Drift

The chopper type of amplifier has a vastly superior temperature drift figure in comparison with the direct coupled differential amplifier.

For the best temperature drift performance, transistors Tr1 and Tr2 should be mounted together in a "Redpoint" heatsink type 92-DC, to keep them both at the same temperature.

No attempt was made to match Tr1 and Tr2 since the values of offset voltage and slope resistance were fairly constant for the several specimens tested.

The temperature drift was found to be approximately $1\mu V/°C$ referred to the input.

SECTION 11

COMPLEMENTARY CIRCUITS

The use of n-p-n and p-n-p transistors in the same circuit can result in simplification of interconnections and a reduction in the number of resistive and capacitive components.

The following circuits illustrate such applications.

Timing Relay Circuit

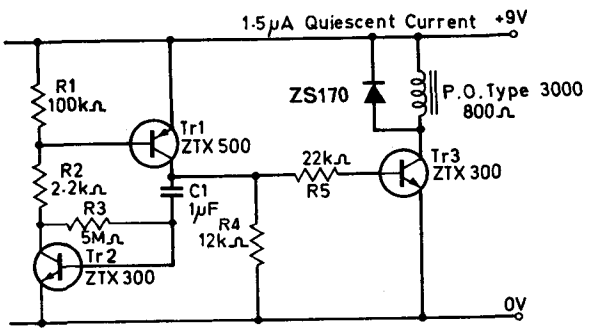


Figure 11.1 (Circuit description overleaf)

With C1 completely discharged, charging current flows in the circuit comprising R1, R2, R3, C1, and R4 components. The voltage across R1 turns on Tr1 and the rising voltage on the base of Tr2 turns this transistor on. As there is a positive feedback loop, both transistors turn on and the capacitor charges, almost to H.T. voltage, very rapidly. As the charging current falls off, a reverse process occurs and both transistors turn off. The top side of the capacitor is tied to earth via R4 and the other side goes negative with respect to earth.

The capacitor discharges to the H.T. line via the 5MΩ resistor R3 giving a 5 second delay. When the base voltage of Tr2 rises above the emitter voltage, the action is repeated. The reverse biased base emitter junction has a typical breakdown voltage of 7·5V and this will limit the negative potential on the base. As the 12kΩ resistor R4 is in the breakdown circuit this is permissible. A positive pulse is applied every 5 seconds to the output transistor Tr3 as transistor Tr1 turns on. With the relay replaced by a 10kΩ resistor a pulse of 3 milliseconds was obtained at the collector. The timing transistors are only conducting during the charging part of the cycle, which makes the circuit very economical in power consumption.

Directly Coupled Amplifier

The circuit uses transistors in a ring of three and demonstrates the high gain that can be obtained with simple circuitry using complementary types, directly coupled.

The voltage gain is 3×10^4, or 90dB.

The high frequency gain is determined by C3, and with the value given, is 3dB at 20kHz. C3 promotes h.f. stability.

The low frequency gain is determined by C1, C2 and the source resistance, resulting in a hump before cut-off. With the values given, the voltage gain rises +4·5dB at 40Hz and falls to –3dB at 25kHz.

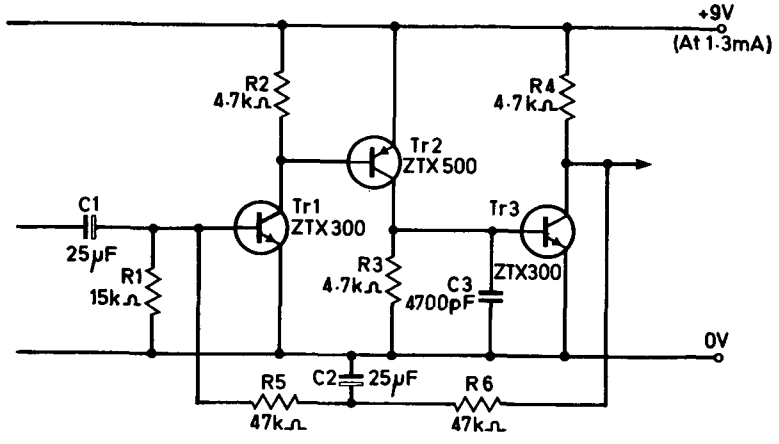


Figure 11.2

The input impedance of Tr2 is

$$r_e \times h_{fe} \text{ in parallel with } \frac{R8}{V.\text{Gain Tr2}}$$

$$= 4{\cdot}5 \times 100, \text{ in parallel with } \frac{47 \times 10^3}{150}$$

$$= 185\Omega$$

Thus, loss due to R5 is:

$$\frac{185}{1185} = 0{\cdot}156$$

Therefore, voltage gain from the junction of VR1/R5 to the output is:

$$0{\cdot}156 \times 150 = 23{\cdot}5$$

Sensitivity at junction VR1/R5 to the output is:

$$\frac{2300}{23{\cdot}5} = 98\text{mV}$$

Tr1 is arranged to operate at 2mA collector current

$$r_e = \frac{27}{2} = 13{\cdot}5\Omega$$

Collector load is 2·2kΩ, 4·7kΩ and 1kΩ in parallel

$$= 600\Omega$$

Therefore, Voltage Gain of Tr1 $= \frac{600}{13{\cdot}5}$

$$= 45$$

and the sensitivity for full output $= \frac{98}{45} \approx 2\text{mV}$

The input impedance is

$$r_e \times h_{fe}, \text{ in parallel with } \frac{100\text{k}\Omega}{V.\text{Gain Tr1}}$$

$$= 13{\cdot}5 \times 100, \text{ in parallel with } \frac{100\text{k}\Omega}{45}$$

$$= 850\Omega$$

Prior to applying the supply voltage, VR2 should be set to zero and subsequently adjusted to give 1mA quiescent currents in Tr3 and Tr4.

The lower frequency limit can be extended to -3dB at 40Hz by increasing C8 to 250μF.

Specification

Supply current with zero output	= 9mA
Supply current at 150mW output	= 40mA
Power output	= 150mW at 10% total harmonic distortion
Sensitivity for 150mW output	= 2mV RMS
Input impedance	= 850Ω
Frequency response	= -3dB at 200Hz and 20kHz

SECTION 12

AVALANCHE PULSE GENERATOR

Figure 12.1 shows the collector emitter voltage breakdown characteristic. If a resistor is connected between base and emitter, the maximum voltage can be increased from $V_{ce(sus)}$ to V_{cer}. If the power is increased further, the collector emitter voltage drops to a low value and there is a sharp increase in collector current. Transistors driven into this secondary breakdown region can be easily destroyed, as the breakdown is due to the collector current being channelled through a small area of the collector base depletion layer. However, if the current is limited in amplitude and duration, use can be made of the very rapid transition into the breakdown region to produce short pulses with high amplitude and fast rise times.

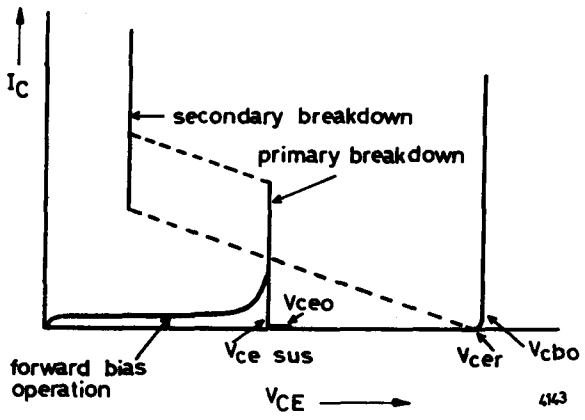


Fig. 12.1

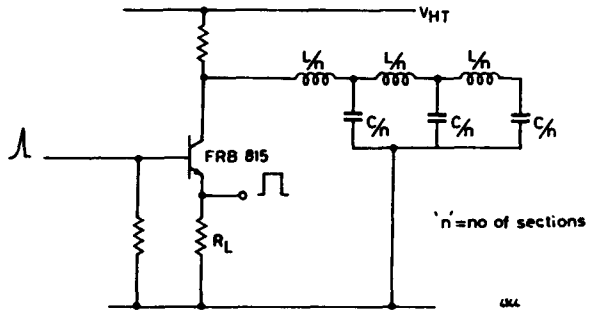


Fig. 12.2

$$\text{Pulse Width} = 2\sqrt{LC}$$

$$Zo = \sqrt{\frac{L}{C}}$$

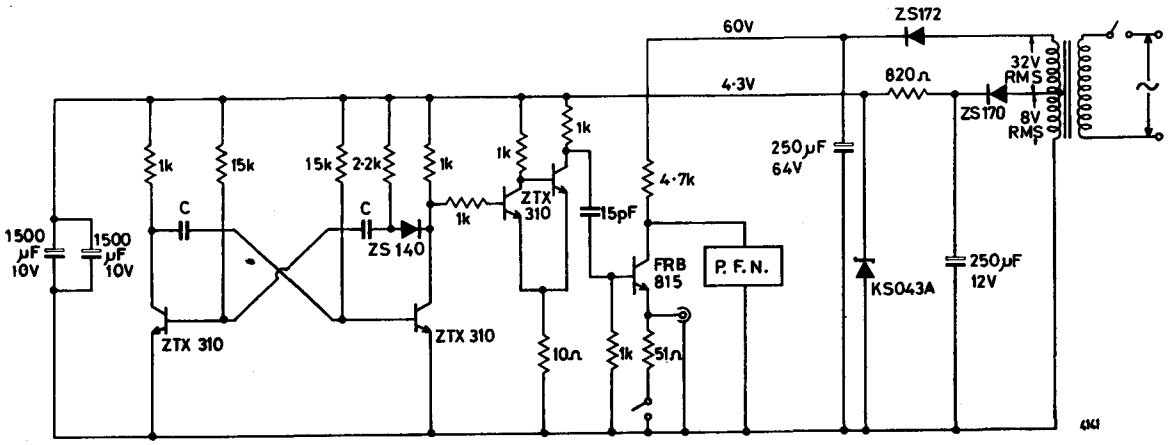
$$V_{ceo} < V_{HT} < V_{cbo}$$

The circuit, Figure 12.2, is shown below the characteristics, and depends upon a charged pulse-forming network or delay line. The capacitance of the network is charged to the HT voltage. On the application of the trigger pulse the transistor breaks down and the network discharges through the transistor and the load. The pulse width is defined by the network. The charging rate, and hence the maximum repetition rate, is defined by the time constant of the collector resistor and network capacity.

A detailed description of secondary breakdown and circuits using this effect can be found in the Application Report " The Use of Transistors in Avalanche Mode "*

* A new Ferranti publication.

Figure 12.3 shows a circuit diagram of a complete pulse generator using an avalanche transistor. A multi-position switch selects the capacitors of a multivibrator circuit which provides trigger pulses with a wide range of repetition rates. A further switch selects the various pulse forming networks to obtain a range of pulse widths. The circuit may be used with either an external 50 ohms load or a built-in load which can be switched into circuit. The output voltage across 50 ohms is 12V.



Switched 'C'	f
4μF	10Hz
0.47μF	100Hz
0.047μF	1kHz
4700pF	10kHz
470pF	100kHz

Pulse Width	Switched P.F.N. (Totals)	Sections
5ns	15pF + 330nH	2
10ns	30pF + 750nH	3
20ns	70pF + 1.5μH	3
50ns	150pF + 3.7μH	4
100ns	300pF + 7.5μH	5

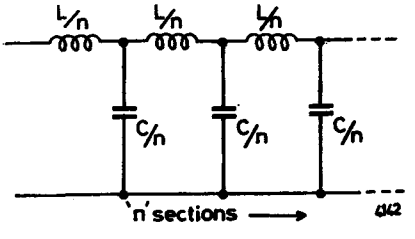


Fig.12.3 — Avalanche Pulse Generator

THE E-LINE PACKAGE is injection moulded with a plastic specially selected to provide a rugged one-piece encapsulation resistant to very severe environments and giving excellent high temperature performance.

Standard lead formation is collector-base-emitter 'in line' (1·27 mm between pins).

ALTERNATIVE LEAD CONFIGURATIONS are available as direct 'plug in' replacements for TO-5 and TO-18 metal can types and are identified by the letters K and L (see outlines below).

The majority of E-Line semiconductors are identified by the letters 'ZTX' followed by the type number.

DIRECT ELECTRICAL EQUIVALENTS are available for the more popular metal can and plastic types and are usually recognised by the type number, e.g.

BC107 = ZTX107L*	BF197 = ZTX197L*
BC213 = ZTX213L*	2N4400 = ZTX4400
BC337 = ZTX337L*	

* *Note:* L = TO-18 lead formation.

THE BASIC PERFORMANCE of E-Line is dependent to a certain degree on the type of chip used in the package. However, the following can be used as a guide.

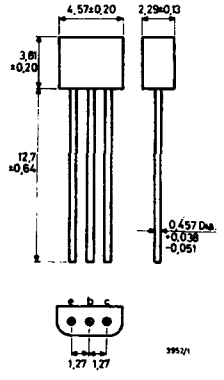
Operating and storage temperature range = **–55** to +175°C

Power dissipation at T_{amb} = 25°C = 200 up to 1000 mW†

Maximum collector current = up to 1 amp†

† Dependent on chip size.

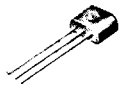
E-Line Plastic Package — Outline & Dimensions

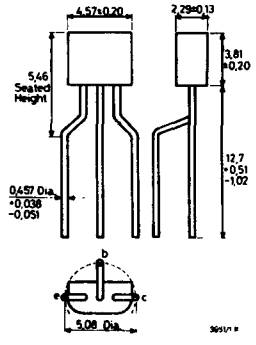


Dimensions in millimetres

STANDARD PACKAGE

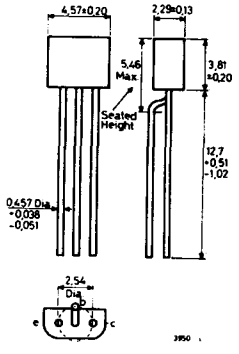
Outline reference
BS3934 .. .. SO-94





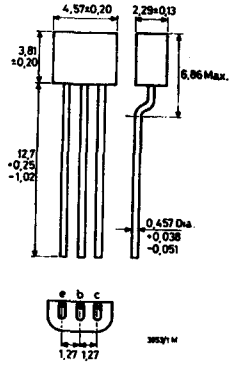
'K' LEAD FORMATION for TO-5 and TO-39 compatibility

Outline reference
BS3934 .. .. SO-95



'L' LEAD FORMATION for TO-18 compatibility

Outline reference
BS3934 .. .. SO-96



'M' LEAD FORMATION for flat mounting

Outline reference
BS3934 .. .. SO-97

Publications

In order to supplement the information given on the data sheets for individual devices, Ferranti Ltd., publish comprehensive information in the form of application notes and reports, brochures, leaflets, etc. These deal with particular devices, or groups of devices, in greater detail and are available on request from the Electronics Sales Department at Gem Mill. Examples of items currently available are listed below.

PRODUCT GUIDES:—

E-Line Plastic Encapsulated Semiconductors.
Opto Electronic Devices.
Semiconductors for Hybrid Circuits.
R.F. & Microwave Power Transistors.
L.F. Power Transistors & Power Rectifiers.
Microwave Diodes.
Integrated Circuits.

BROCHURES:—

ESA 39 A VHF/FM Receiver Design.
ESA 41 A Six Channel Digital Proportional Radio Control System.
ESB 45 E-Line Transistor Applications. (Price 40p).
ESB 57 CDI — The Bipolar LSI.
ESB 62 ULA — The Uncommitted Logic Array.
ESB 63 Low Power TTL (LTTL).

APPLICATION REPORTS:—

No. 8 Voltage Regulators and Reference Diodes.
No. 11 Microlin Amplifiers ZLD2S and ZLD2T.
No. 13 R.F. Power Circuits using Ruggedised R.F. Power Transistors.
No. 14 Silicon Opto-Electronic Devices.
No. 15 ZN402 — The Gated Operational Amplifier.
AR/121 ZN414 — The One Chip Radio Receiver.

APPLICATION NOTES:—

No. 12 Voltage Transient Protection of Silicon Rectifiers.
No. 14. Silicon Rectifiers in High Voltage Applications.
No. 23 The Controlled Avalanche Rectifier: General and High Voltage Applications.
No. 24 10kV Stabilised EHT Supply using Silicon Transistors.
No. 32 1kW D.C. Amplifier.
No. 35 Micro-E Transistors Thermal Ratings and Mounting Techniques.
No. 37 A Low Power High Efficiency Output Stage using ZT3866 Transistors.
No. 38 A Low Q Bandpass Amplifier Design using ZT3866 Transistors.
No. 39 A V.H.F. Ring Divider.

LEAFLETS:—

ESB 53 Micronor 2 DTL, Series 300E or 300HE.
ESB 59 Micronor 2 DTL, Series 200E.
ESB 60 Micronor 2 DTL, Series 110 and 130
ESB 62 Micronor 2 DTL, Series 200 and 300.
ESA 43 Performance Assessment of a Range of Plastic Encapsulants and Device Manufacturers.
ESA 46 Environmental and Reliability Assessment of Micro-E devices.

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DELIVERY ENQUIRIES 061-624 6661 Ext. 290

Information on the current delivery position of any of our range of products will be given by members of our staff who attend to these questions personally.

TECHNICAL ENQUIRIES AND QUOTATIONS 061-624 6661

In the Electronic Sales Department we have a staff of engineers who are able to furnish you with price quotations and with technical advice on problems relating to your individual requirements. These engineers are assigned to specific areas and are thus familiar with many of your companies needs. They are also in constant touch with our **Field Sales Engineers** who will be pleased to call upon you to discuss your semiconductor requirements.

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The distributor's area is not limited to his geographical location.

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Baillie Street,
Rochdale.
Telephone: 0706 47411
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Coronet House,
Upper Well Street,
Coventry CV1 4AF.
Telephone: 0203 21051
Telex: 311243

Swift Hardman Limited,
Swift House,
Liverpool Road,
Newcastle-u-Lyme,
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